PRODUCTION ENGINEERING MEASURE FOR AN INTEGRATED CIRCUIT POWER AMPLIFIER 600-1000 MHz, FOR TACTICAL RADIO EQUIPMENT

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This program was directed towards developing and establishing techniques for manufacturing broadband high power UHF amplifiers. Specifically, a 30 watt amplifier that covered the 600 to 1000 MHz instantaneous bandwidth was to be produced.

The work involved; 1) design and characterization of transistors; 2) optimization of internal transistor matching networks; 3) design and fabrication of broadband impedance matching circuits; 4) study and design of broadband power splitters/combiners; 5) batch fabrication of microstrip circuits on alumina; 6) mechanical

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package design; 7) development of amplifier assembly techniques. During the program a number of engineering models were fabricated and tested prior to the production run. The production amplifiers incorporated changes based on the perfor. nce of these engineering models. Elect-ical, mechanical and environmenta1 tests were performed as required by the specifications.

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SECTION I - INTRODUCTION

The objective of this production engineering measure was to establish a production capability for manufacturing broadband, highly reliable, integrated circuit amplifiers for use in Army communications equipment.

The work involved; 1) design and characterization of transistors; 2) optimization of internal transistor matching networks; 3) design and fabrication of broadband impedance matching circuits; 4) study and design of broadband power splitters/combiners; 5) batch fabrication of microstrip circuits on alumina; 6) mechanical package design; 7) development of amplifier assembly techniques. During the program a number of engineering models were fabricated and tested prior to the production run. The production amplifiers incorporated changes based on the performance of these engineering models. Electrical, mechanical and environmental tests were performed as required by the specifications.

The accomplishment of the task involved in this contract was done with the guidance and support of Mr. Dave Biser, Project Engineer, and Mr. Russell Gilson, Laboratory Engineer, at the U. S. Army Electronics Command, Fort Monmouth, New Jersey.

Reports and other information procured under this requirement will be used for industrial mobilization and preparedness planning to determine what additional planning measures are required, and when necessary, to assist in establishing additional sources.

SECTION II - TECHNICAL NARRATIVE

2.0 INTRODUCTION

This program was directed towards developing and establishing production techniques for manufacturing broadband, high power UHF amplifiers. Specifically, an amplifier that produces an output power of 30 watts over the 600 to 1000 MHz instantaneous frequency band was to be developed. A single stage 18 watt amplifier was designed and two of these amplifier stages were power combined to realize the 30 watt output capability.

Low cost amplifier production depended on the ability to produce broadbandable transistors and matching circuits that required little or no tuning. The internal matching network incorporated in the transistor package was optimized for the 600 to 1000 MHz operating bandwidth thus facilitating broadbanding. The input and load matching networks were computer designed. The power splitter/combiner and the matching networks for the complete 30 watt amplifier were batch fabricated using microstrip on 2 x 2 inch alumina substrates to minimize cost. Manufacturing processes and process controls were developed for batch processing the 2 x 2 inch substrates. Techniques for assembling the amplifier and hermetically sealing the package were investigated and developed.

To demonstrate the combinability of the completed amplifier module, four amplifier modules were power combined to produce 100 watts.

2.1 POWER SPLITTER/COMBINER INVESTIGATION

During the course of this contract, techniques for power combining a pair of transistor amplifiers were investigated. Both the quadrature hybrid and push pull 180° type of combiners were studied. An interdigitated quadrature hybrid combiner originally developed by Lange was chosen. This type of combiner could be realized in

microstrip form and could be fabricated simultaneously with the microstrip matching networks, thus facilitating batch processing. In addition, this type of combiner provides isolation between the pair of amplifiers being combined and can be designed to operate over a full octave of bandwidth.

The use of push pull 180° power combiners was also investigated because it offered to reduce second harmonic content of the amplifier output power.

2.1.1 Push Pull Combiner Structures

A push pull combiner takes an input signal and splits it into two equal parts 180° out of phase. A balanced to unbalanced conversion must also be made if it is desired to interface with standard 50 ohm coaxial systems. The coupled transmission line configuration shown in Figure 1, provides both the 180° phase difference between outputs and the balun action needed.

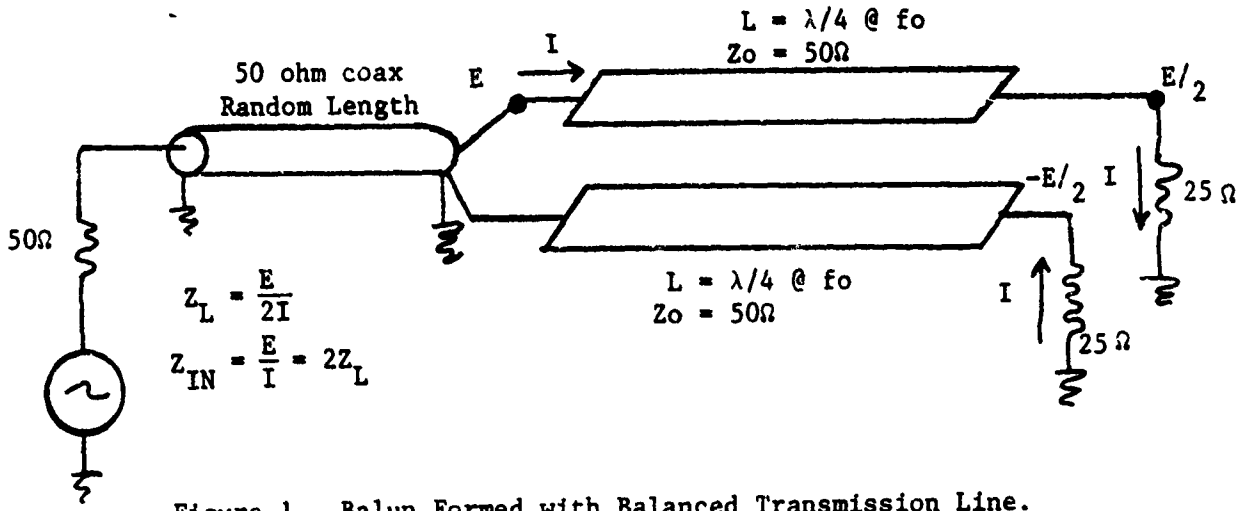


Figure 1. Balun Formed with Balanced Transmission Line.

Because one end of one of the conductors forming the balanced transmission line is connected to ground, no potential is applied to that part of the transmission line. Any power appearing at the other end of that conductor appears there through the mutual coupling that exists between the two conductors. The unbalanced current induced by the -E/2 potential at the output end of the grounded line is choked off, because the line is one quarter wave length long and the ground short is translated through that length as an open circuit. The coupled line configuration is of interest because it can be formed on a substrate which lends itself to batch processing. The coupled line configuration can be implemented in microstrip by etching a line on each side of the substrate.

A coaxial balun is shown in Figure 2.

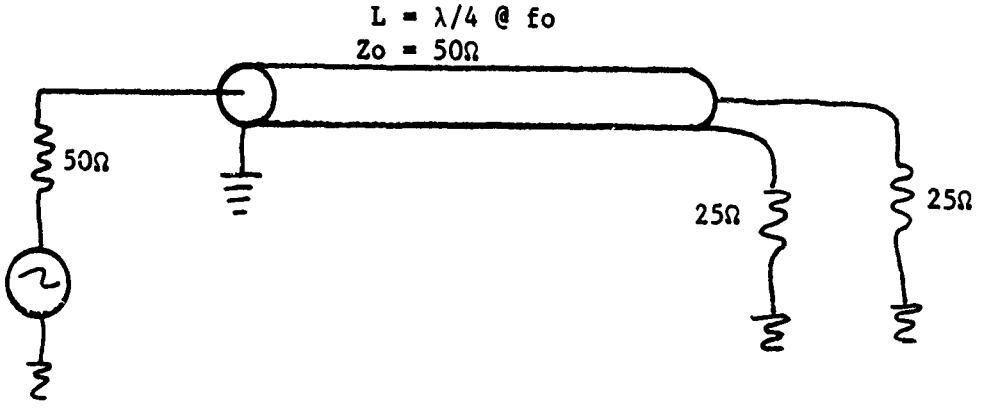


Figure 2. Coaxial Balun.

The coaxial balun was of interest due to the complete containment of the center conductor by the outer conductor, totally containing the field and providing 100 percent coupling. This feature is not provided by the parallel coupled line balun due to fringing effects which exist in any non-totally enclosed transmission line. Note that both

baluns as configured provide a two to one impedance transformation reducing the amount of matching required between the transistor chip and the balun.

2.1.2 180 Degree Balun Coupler Evaluation

Both parallel line and coaxial baluns were investigated. The one-quarter wavelength parallel line balun produced very disappointing results. Figure 3 shows the amplitude errors measured in both a parallel line and a coaxial balun. Note the severe amplitude unbalance over portions of the frequency range in the parallel line balun. This was caused by the fringing capacitance coupling energy to external conductors. The curve could be influenced by loading the ground strips around the edges of the balun.

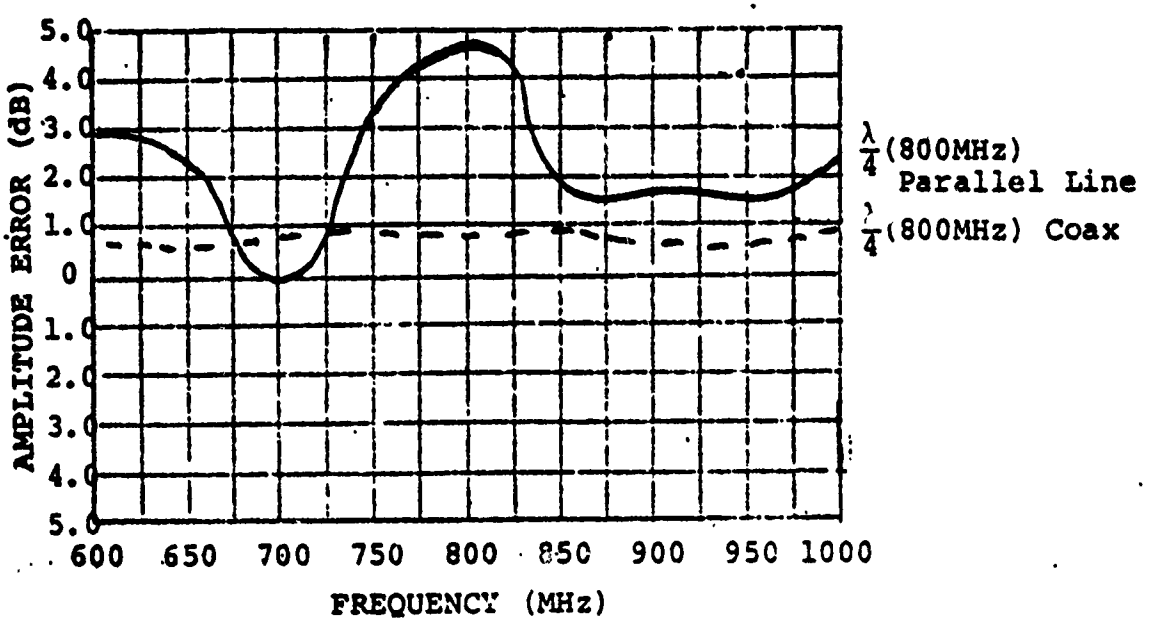


Figure 3. Amplitude Unbalance Vs Frequency for a Parallel Line and for a Coaxial Balun.

Note: The amplitude error is defined as the difference in output power magnitude between the two output ports.

The better performance of the coaxial balun can be attributed to two phenomena. Fringing effects in the parallel line coupler reduce the coupling between the two conductors of the parallel line. This effect is not noted in the coaxial line because the outer conductor completely encloses the inner conductor. In both baluns the load connected to the grounded conductor is shunted by the inductance and stray capacitance from the load end of the conductor to ground. Therefore, a parallel current flows down this conductor. As no such current exists in the conductor connected to the hot end of the generator, an unbalance exists between the two load ports of the balun. The coaxial transmission line minimizes the effects of this unbalance because the Z_o of the coaxial shield to ground can be maximized more readily than can that of the larger microstrip conductor.

Figure 4 shows the effects of type 1Z2 ferrite loading of various lengths applied to the one-quarter wavelength coaxial balun. In each case the ferrite was positioned at the output end of the coaxial line and the outside conductor was shorted to ground at the end of the ferrite loading. The short minimizes the effects of stray capacitance from the unloaded section of line.

Figure 5 shows the results obtained when type CN11 ferrite loading was used to choke out the unbalance current on the coaxial line. Again the ferrite was positioned at the output end of the balun and the output conductor was shorted to ground at the end of the ferrite loading.

To illustrate the effects of stray capacitance, the transformer used to obtain the data in Figure 5 was modified to increase the spacing between the coaxial line and ground. All other parameters were held constant. Note improved balance at higher frequency obtained by reducing the stray capacitance as shown in Figure 5.

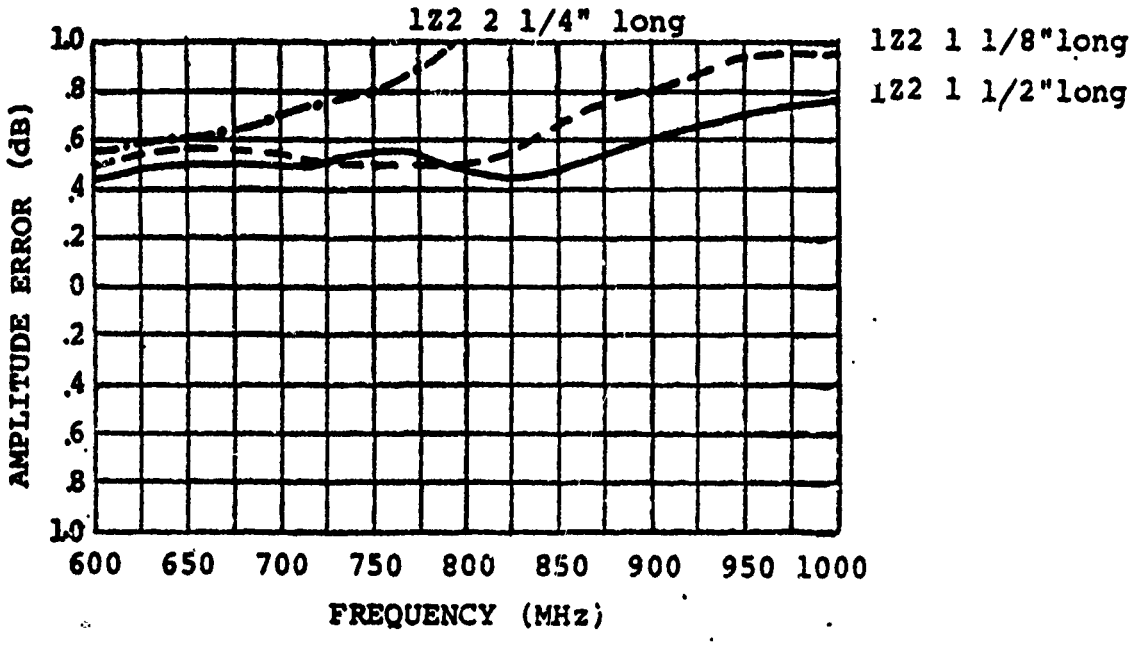


Figure 4. Balun Coupler Amplitude Balance Vs Frequency For Various Amounts of Type 1Z2 Ferrite Loading.

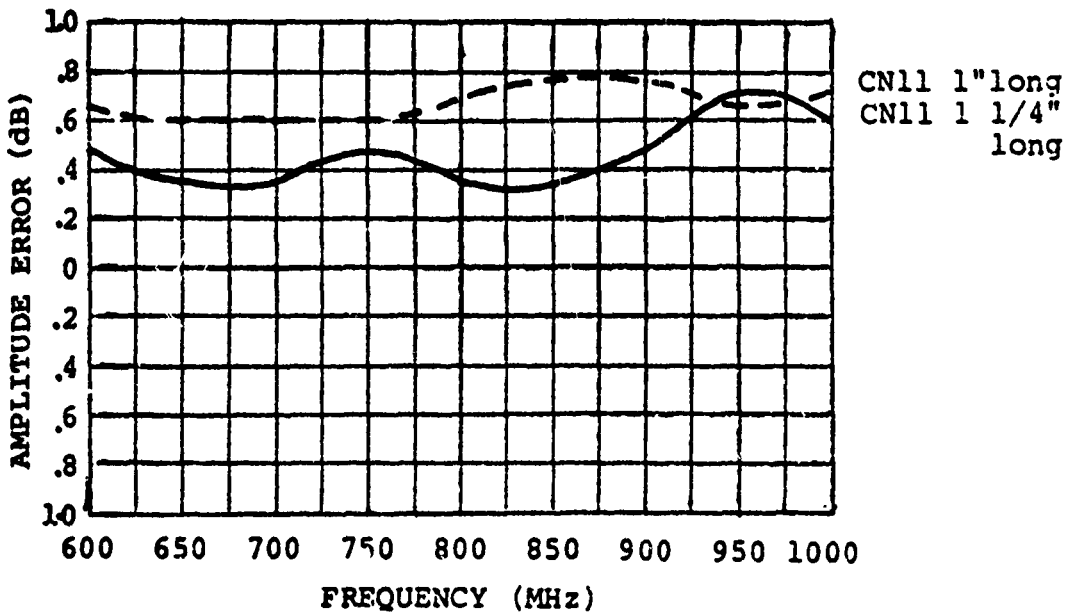


Figure 5. Balun Coupler Amplitude Balance Vs Frequency For Various Amount of Type CN11 Ferrite Loading.

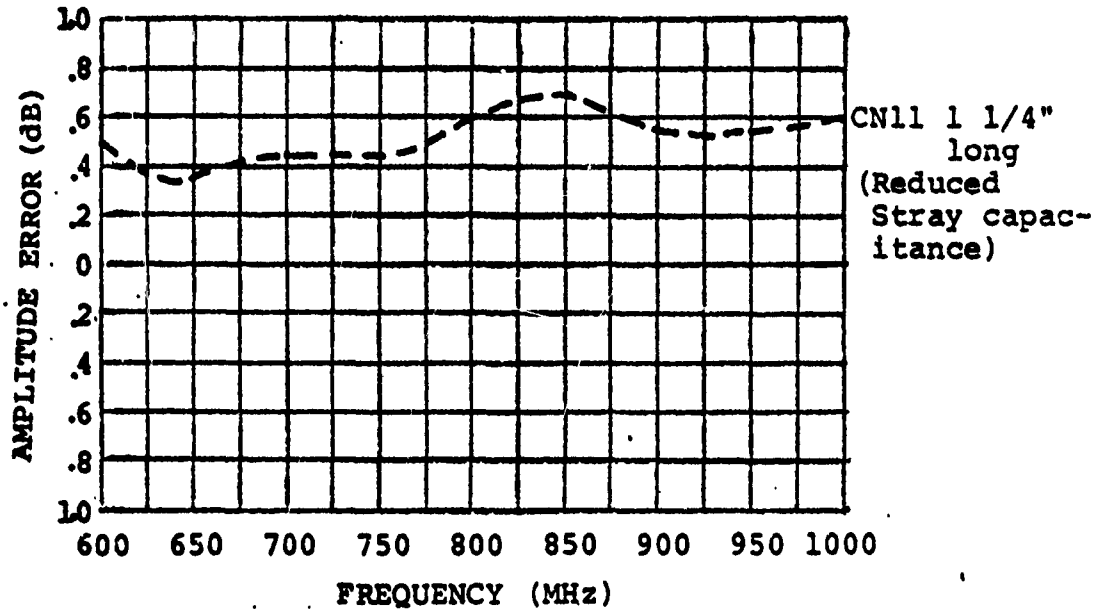


Figure 6. Balun Coupler Amplitude Balance Vs Frequency For Type CN11 Ferrite Loading When Stray Capacitance is Reduced.

To further increase balance, the couplers were redesigned. As it appeared from the previous data that little benefit was derived from increasing the ferrite loading beyond one and one-quarter inches to one and one-half inches, the coaxial line was shortened to just allow this amount of loading. Also, an additional ferrite loaded coaxial line of the same length was connected to the center conductor of the balun. (See Figure 7.) This added conductor introduces an unbalance current to the center conductor which is equal to the unbalance current in the outer conductor. Thus, balance is improved. Care must be taken to insure that both "pipes" have the same amount of ferrite loading and the spacing to ground is the same. In addition, interconnecting lead inductance must be held to an absolute minimum. Figures 8 and 9 show the balance data obtained from both 1Z2 loading and CN11 loading. The phase data obtained and presented may not be completely accurate. Different readings were obtained when the vector voltmeter probes were interchanged. Therefore, the phase data presented in Figure 9 was averaged from the two sets of readings. The worst case error measured at any frequency with any vector voltmeter probe connection was less than 10 degrees so large deviations from the presented data are not expected. The amplitude unbalance data was obtained from a power meter which was moved from output port to output port. The output port not being measured was terminated in a precision dummy load. The insertion loss for both types of ferrite loaded baluns is shown in Figure 10. The irregular shape of these curves indicates that all loss may not be dissipative in nature (some may be due to reflections causing some input power to be reflected to the generator rather than dissapated in the cores or conductors of the coaxial lines). Impedance measurements (Figures 11 and 12) taken on the two types of ferrite loaded transformers tend to validate this conclusion. Note that where the 1Z2 loaded transformer exhibits a peak insertion loss at

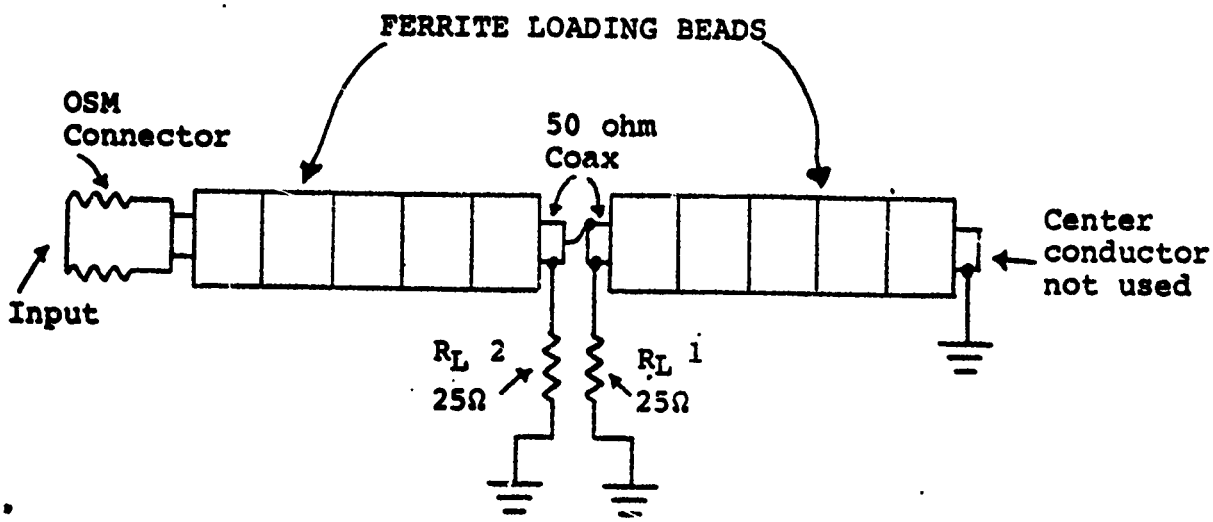


Figure 7. Improved Balun Construction.

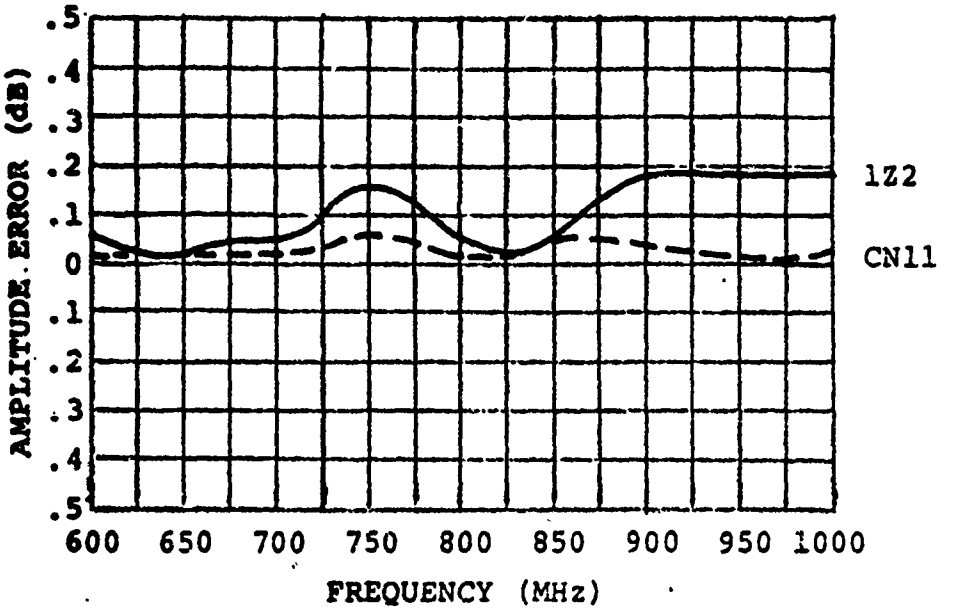


Figure 8. Amplitude Unbalance for Two Ferrite Loaded Baluns.

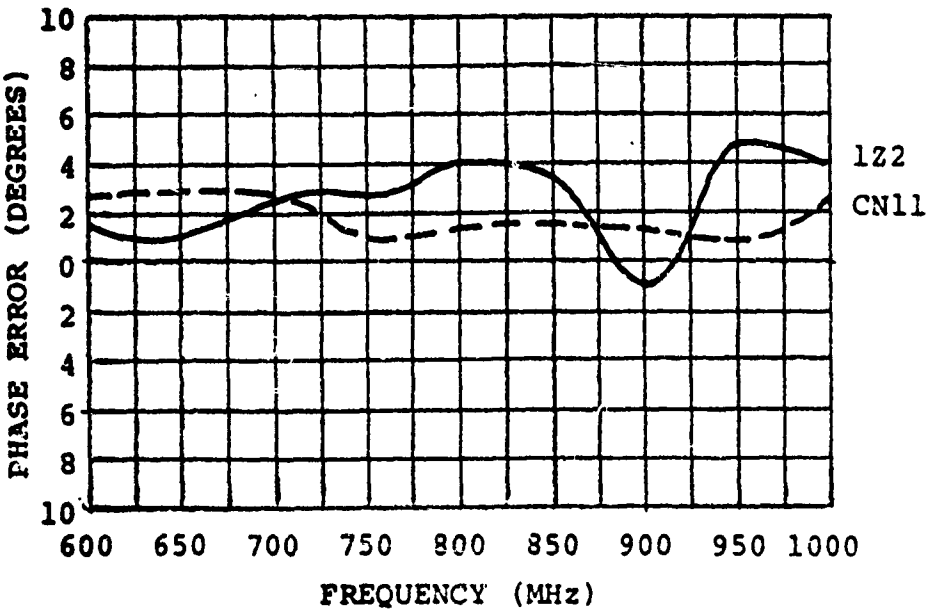


Figure 9. Phase Unbalance for Two Ferrite Loaded Baluns.

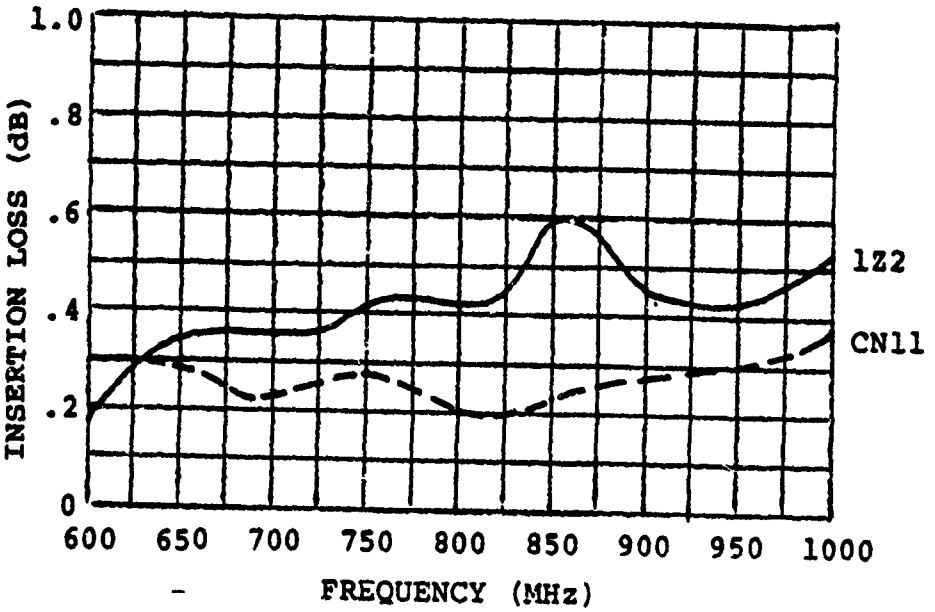
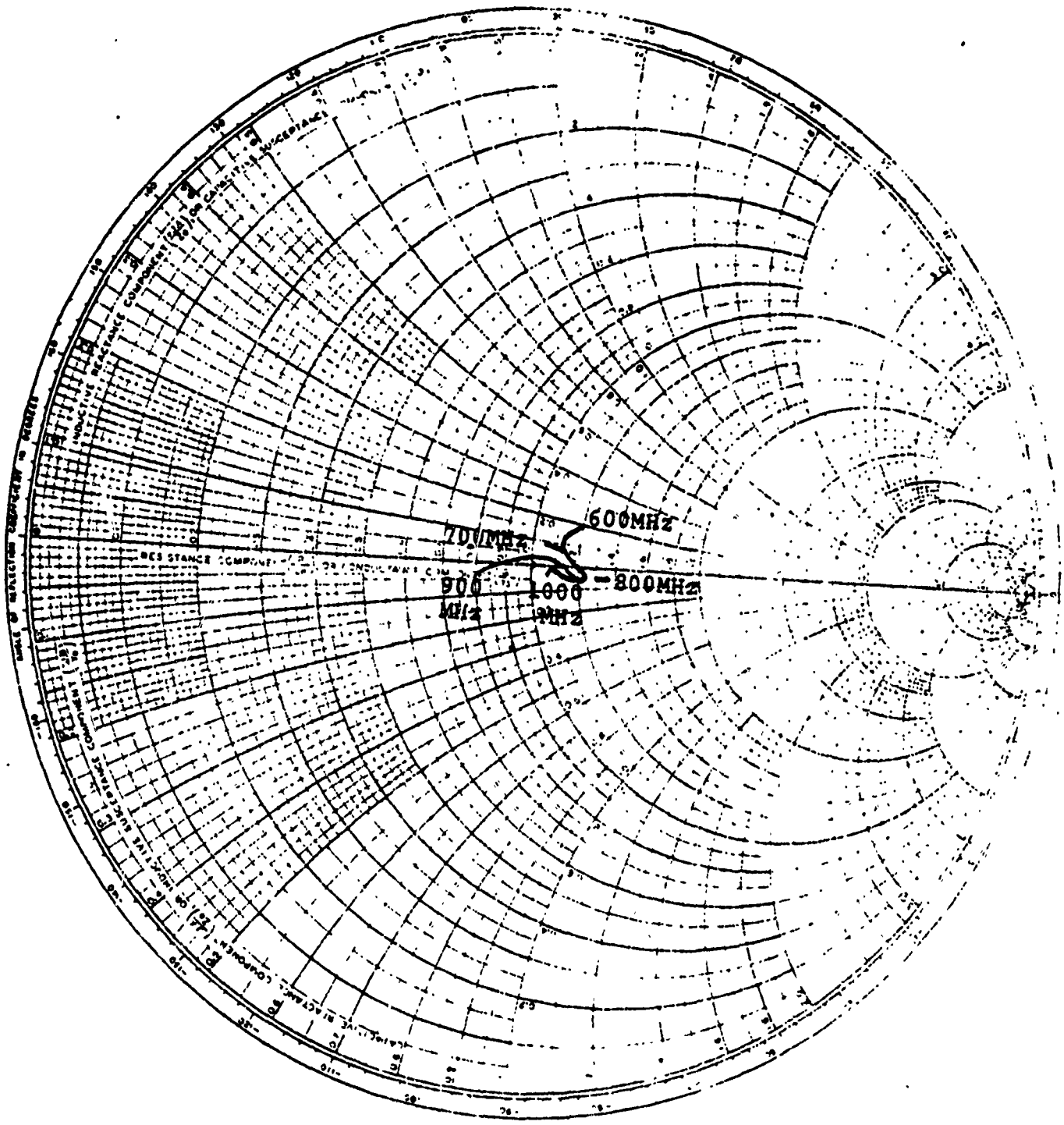
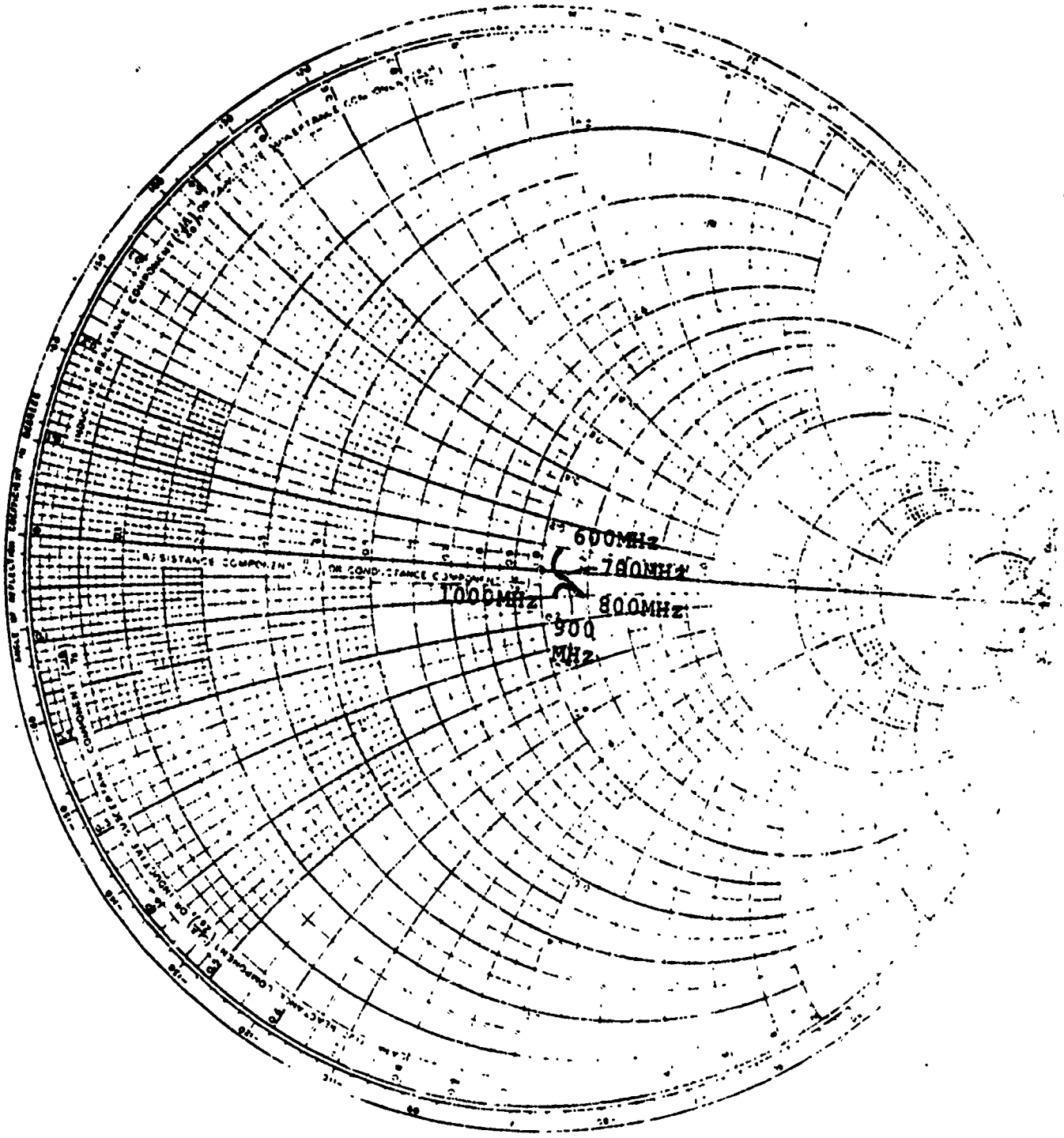


Figure 10. Insertion Loss for Two Ferrite Loaded Baluns.



Zo = 50Ω

Figure 11. Impedance of Balun Made with CN11 1 1/4" Long Loading.



Zo = 50Ω

Figure 12. Impedance of Balun Made with 4-1Z2 Beads for Loading.

800 MHz is also where its VSWR is a maximum. Also, note that the higher loss at 600 MHz in the CN11 loaded transformer corresponds to a higher VSWR for this transformer at this frequency. Correcting the insertion loss data for VSWR does not significantly alter the test results due to the low VSWR involved. The CN11 type material exhibits slightly better performance characteristics as indicated in Figure 9.

At this point, the two transformers were connected back to back as shown in Figure 13. The output of the two baluns was terminated in a precision dummy load and impedance data was taken. (Figure 14.) To verify that the baluns were indeed performing, the connections were then changed so that the center conductor of the input balun was then connected to the outside conductor of the output balun. This data is shown in Figure 15. Note the excellent correlation between the two impedance plots. Balance was further verified by connecting the two output ports of the input balun together. If these ports are equal in amplitude and 180 degrees out of phase complete reflection of all input power should occur. Any deviation from balance will result in the input impedance deviating from the periphery of the Smith chart and moving towards the center of the chart. Figure 16 shows the results of this experiment. Figure 17 and 18 are photographs of the parallel line balun. Figure 19 is a photograph of one of the coaxial baluns tested during this effort.

2.1.3 Balun Coupler Conclusions

From the previous investigation it was determined that an effective balun coupler would be much larger than previously expected. The coupler would be influenced by surrounding metallic objects which is not totally compatible with the batch processing goals of the contract. A conference was held with ECOM personnel (R. Gilson) and it was mutually decided to investigate the feasibility of changing the balun coupler to a 90 degree hybrid coupler.

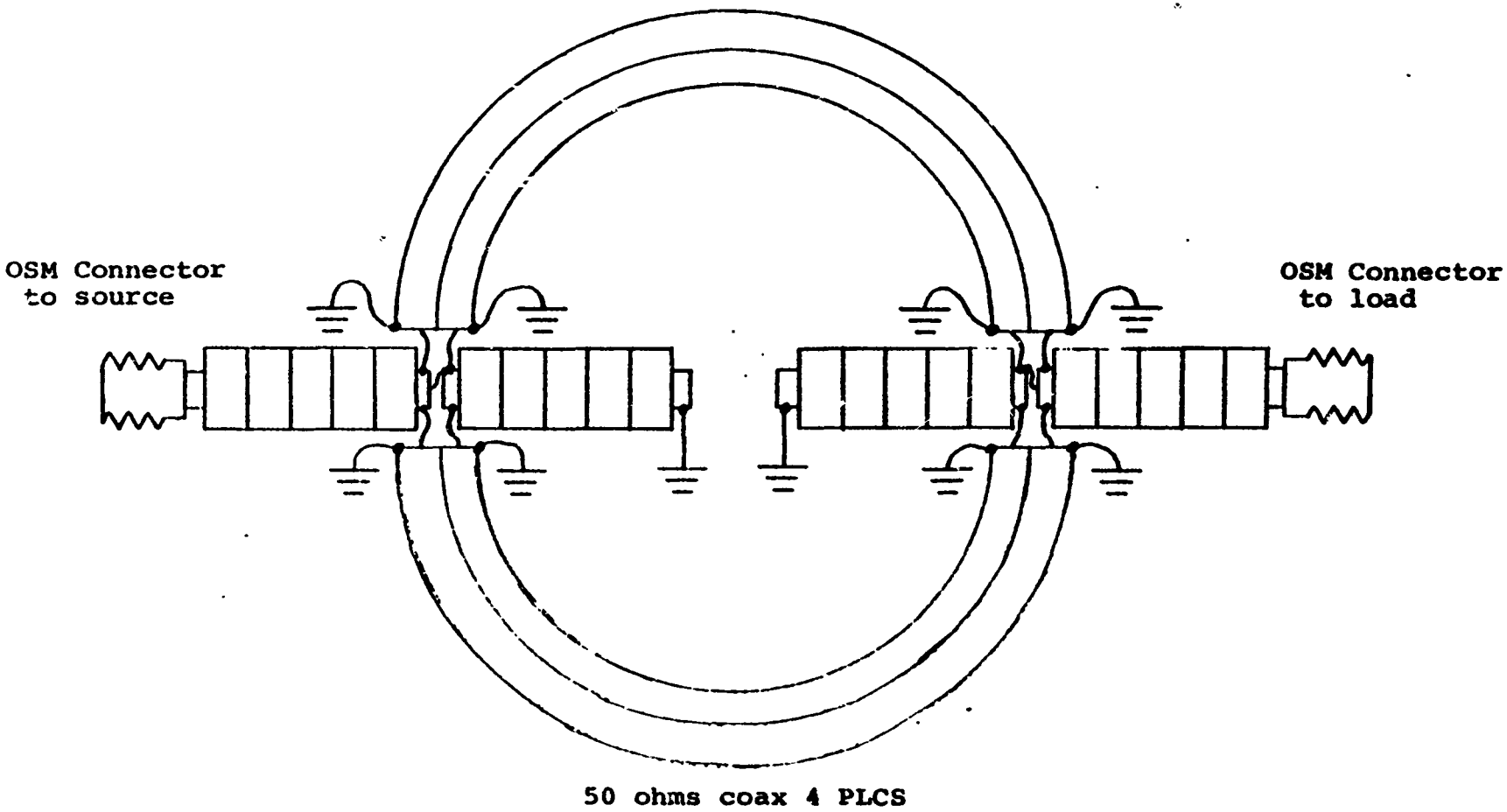


Figure 13. Two Balun Connection For Impedance Testing.

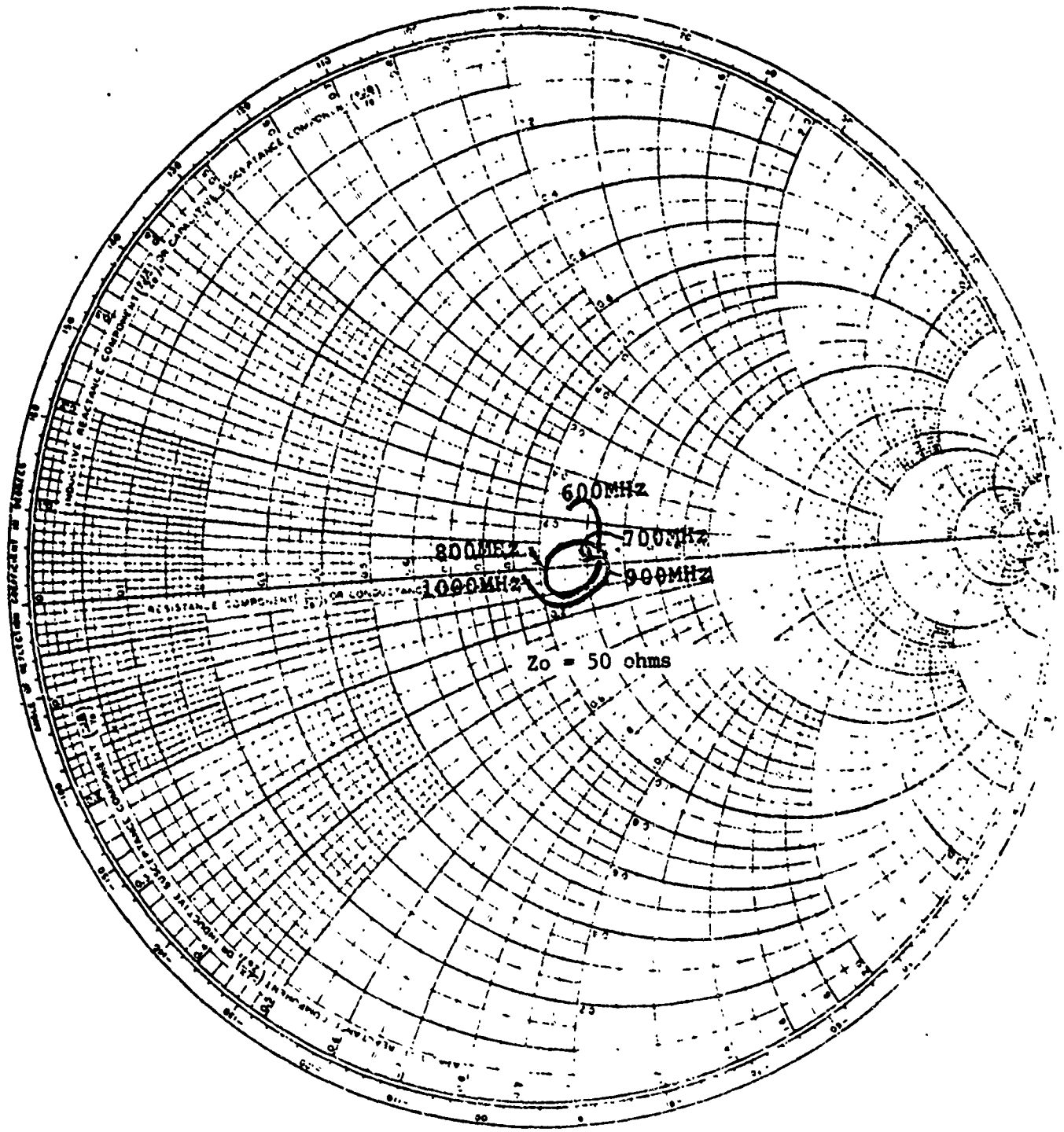


Figure 14. Input Impedance of 2 Baluns Connected as shown in Figure 13.

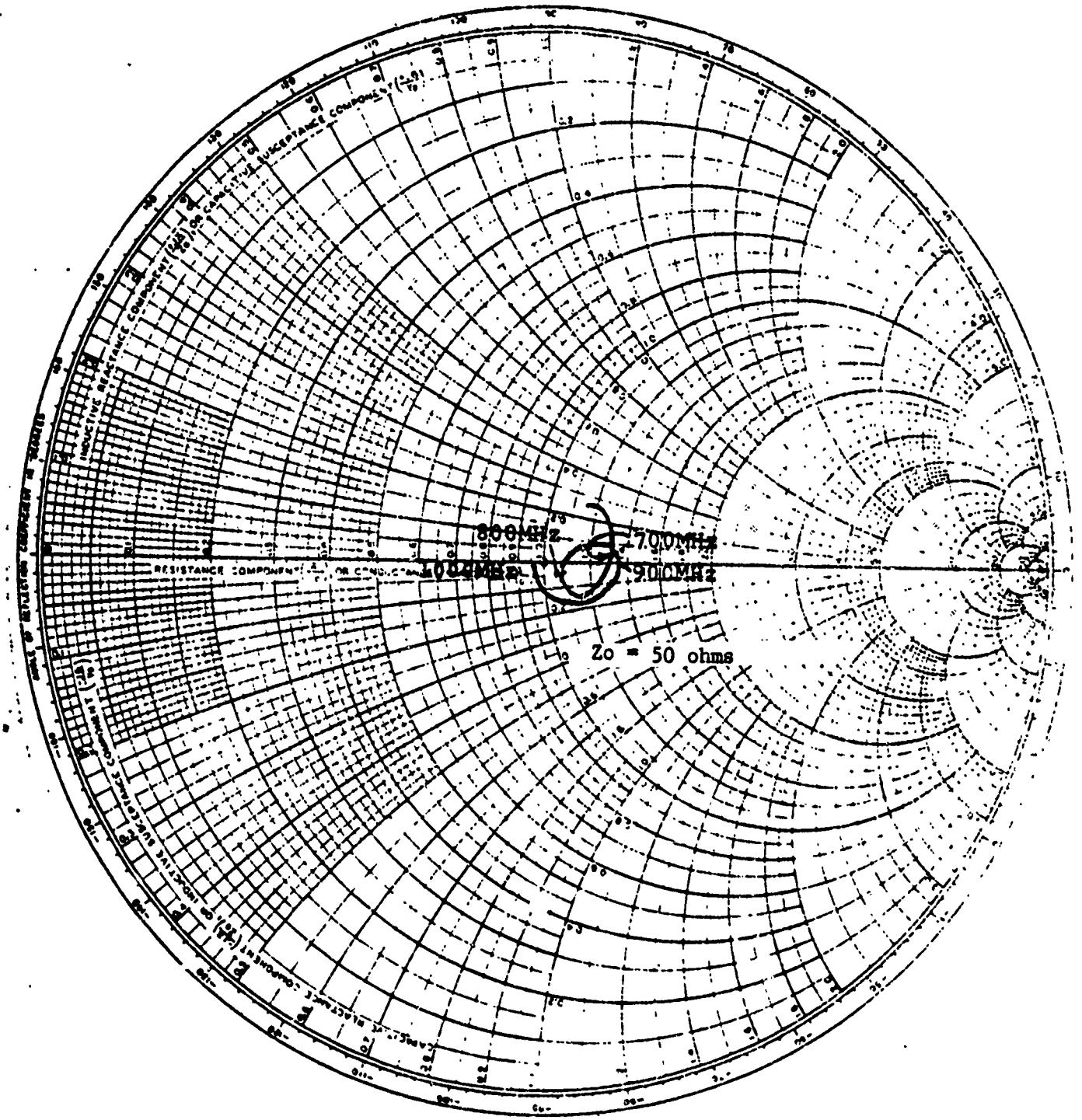


Figure 15. Input Impedance of 2 Baluns with the Connections to the Output Balun Reversed from the Configuration shown in Figure 13.

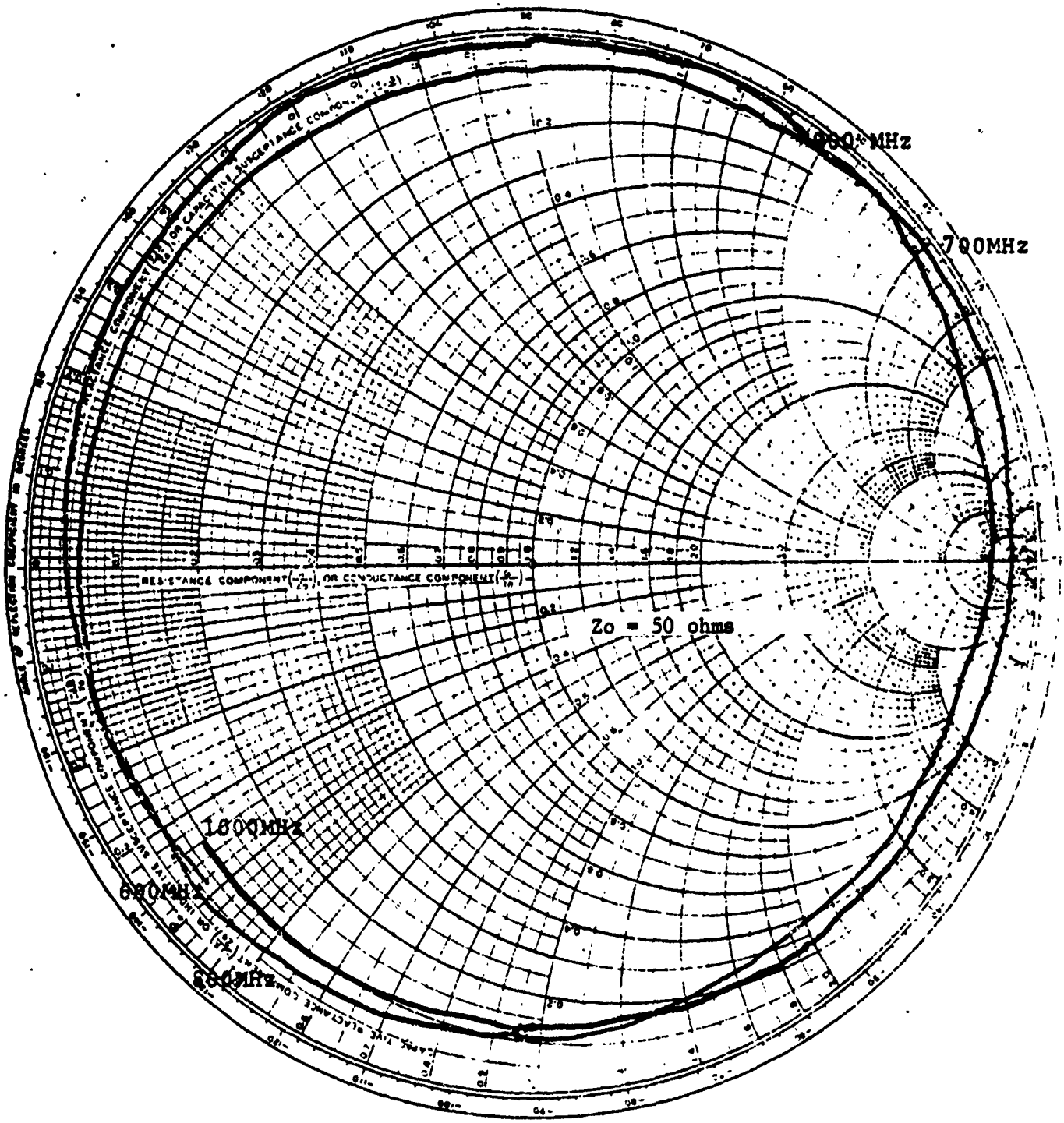


Figure 16. Input Impedance of a Balun Transformer Connected for Cancellation.

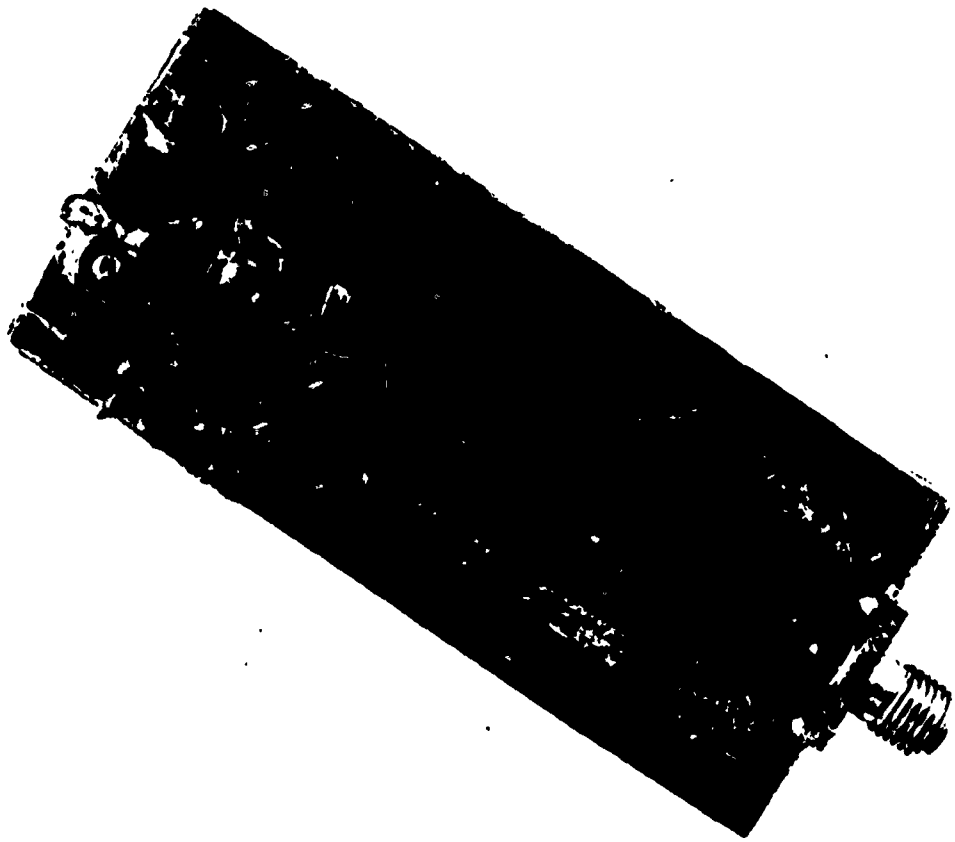


Figure 17. Parallel Line Balun Coupler (Top View).

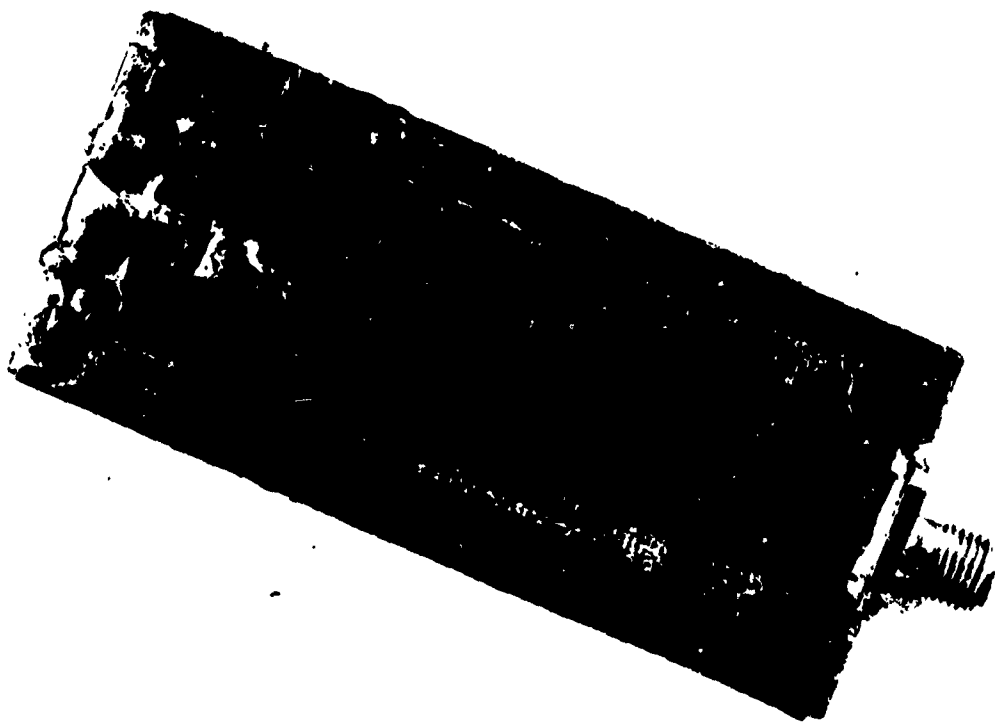


Figure 18. Parallel Line Balun Coupler (Bottom View).

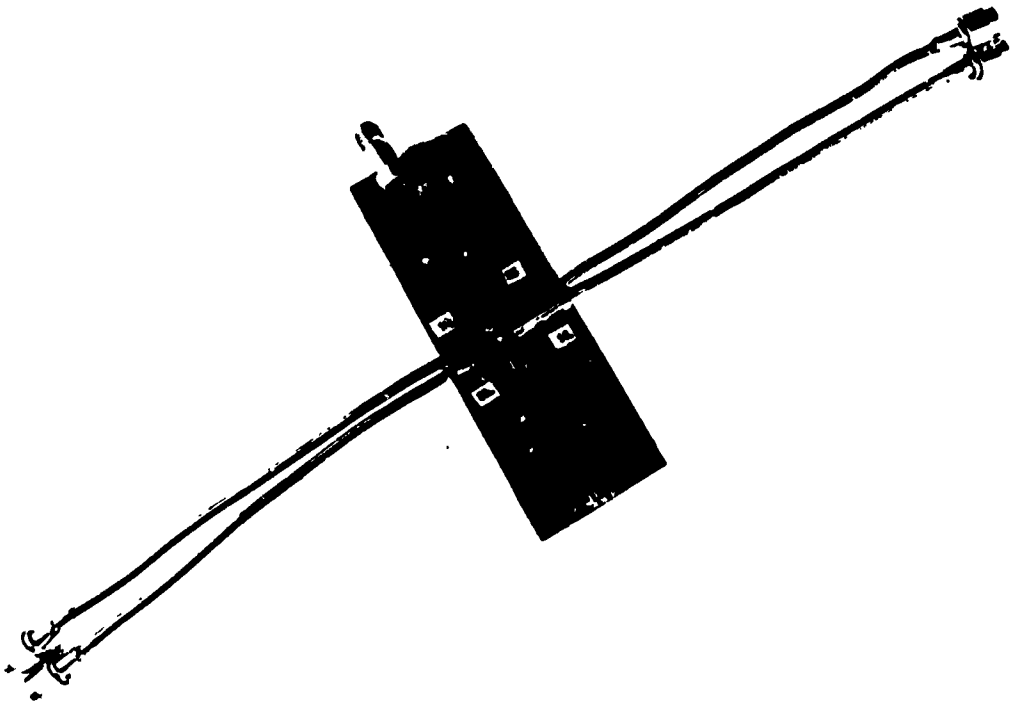


Figure 19. 180 Degree Ferrite Loaded Coaxial Balun Coupler Photograph.

2.2 90 DEGREE HYBRID EVALUATION

2.2.1 Hybrid Selection Criterion

The hybrid selected for evaluation should provide adequate bandwidth for covering the full 600 MHz to 1000 MHz frequency range. It should also provide an equal power split, maintain a 90° phase difference between the output ports, and exhibit good isolation between output ports. For batch processing capability, a microstrip coupler would eliminate the need for sandwitching dielectrics and avoid the necessity for microstrip to stripline conversions. Small physical size would assist in minimization of amplifier physical dimensions and might allow the use of a single substrate for processing all matching circuitry and couplers thus eliminating interconnections.

Considering the above requirements the interdigitated or Lange coupler was selected for investigation.

2.2.2 Hybrid Design

Design of the quadrature couplers was initiated by characterizing the quadrature couplers developed for the broadband combinable power amplification contract (DAAB07-72-C-0042). The measurements indicated that the line width to line spacing ratio (W/S) of this coupler was 1.5 which was correct for providing one octave of bandwidth. By using the same aspect ratio so that the coupling characteristics could be maintained, it was possible to scale the coupler to the lower center frequency by a change in length only. The coupler developed under contract DAAB07-72-C-0042 was for optimum performance over the 1.35 GHz to 1.85 GHz frequency range. It had a length of 0.800 inches and a W/S ratio of 1.5. Characterization of this coupler over the octave frequency range of 1.1 GHz to 2.2 GHz proved that the aspect ratio (W/S) was optimum for an octave range coupler. The center frequency of this coupler was

$f1\left(\frac{fh}{f1}\right)^{1/2}$ or 1.1 $(2.2/1.1)^{1/2}$ or 1.56 GHz. The center frequency of the .550 GHz to 1.1 GHz frequency range was $f1(Fh/F1)^{1/2}$ or $.55(1.1/.55)^{1/2}$ or .779 GHz. Lengthening the coupler by the factor of 1.56/.779 = 2.0 provided the final design. The alternative to this procedure was starting from published design equations and was rejected because it was felt that the measured data was a better starting point as theoretically ignored strays were accommodated by the measured data. Figure 20 shows a layout of the coupler artwork. The coupling is provided by the three mil microstrip lines spaced two mils apart. Bond wires located at the ends of each line, arching over the adjacent line to the next line complete the coupler.

2.2.3 Substrate Material Problems

It was initially desired to use alumina superstrates for best physical definition of the hybrid. Several batches of superstrates were processed and adequate metal adhesion was never obtained. Because excessive substrate binder material on the substrate surface was suspected, a possible solution to this problem appeared to be the use of ground and polished substrates. The grinding process produces a substrate that has much less warpage than a fired substrate and with the polishing operation any desired surface finish can be achieved. Attempts to manufacture hybrids on this material brought out two problems. The grinding process tore large pieces of alumina from the substrate which left holes in the polished surface as large approximately two mils in diameter. These holes were sputtered with both cermet and gold which was virtually impossible to etch out, porducing both electrical shorts and poor coupler definition. In addition, the holes produced stress concentrations in the substrate which made scribing and breaking very difficult. Finally, the decision was made to try a fired alumina material and evaluate the coupler performance.

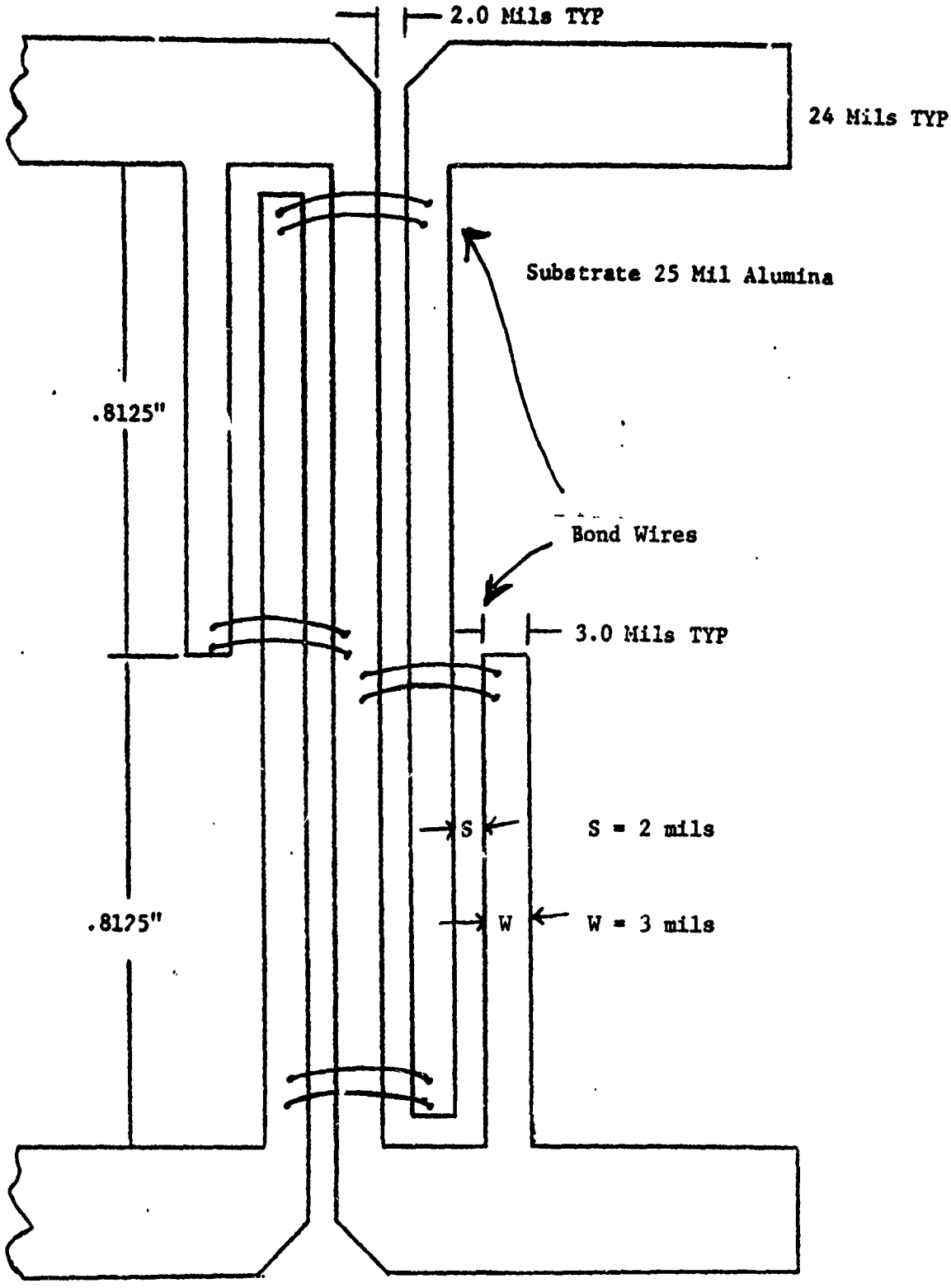


Figure 20. Interdigitated Quadrature Coupler Drawing.

2.2.4 Test Results, Interdigitated Quadrature Couplers

A batch of substrates were fabricated for evaluation of quadrature couplers. These quadrature couplers were built on the ground and polished alumina. The quadrature couplers were cut from the substrates witha diamond saw to preclude any possibility of coupler breakage. The couplers were mounted to a brass block using indium solder and coaxial connectors were attached to the four external ports. A precision load was attached to the difference port. The test results are shown in Figures 21 through 24. It should be noted that the insertion loss indicated by Figures 21 and 22 is slightly higher than will be experienced in the finished amplifier module due to the extra connectors necessary for testing purposes. Past experience has shown this loss to be approximately 0.1 dB. When the connector loss is subtracted from the total loss, the coupler loss is in the 0.3 to 0.4 dB range at 1000 MHz. The bulk of this loss is metal loss due to insufficient skin depth (δ)

$\delta = (6.61/f^{1/2})K$ (cm) = 5.1×10^{-4} cm = 5.1 μm, K = 2.44 for gold.

A minimum of three skin depths is required to provide truly low loss conductors. A reduction in insertion loss is not felt to be practical because these couplers were plated to a thickness of 7 to 8 microns.

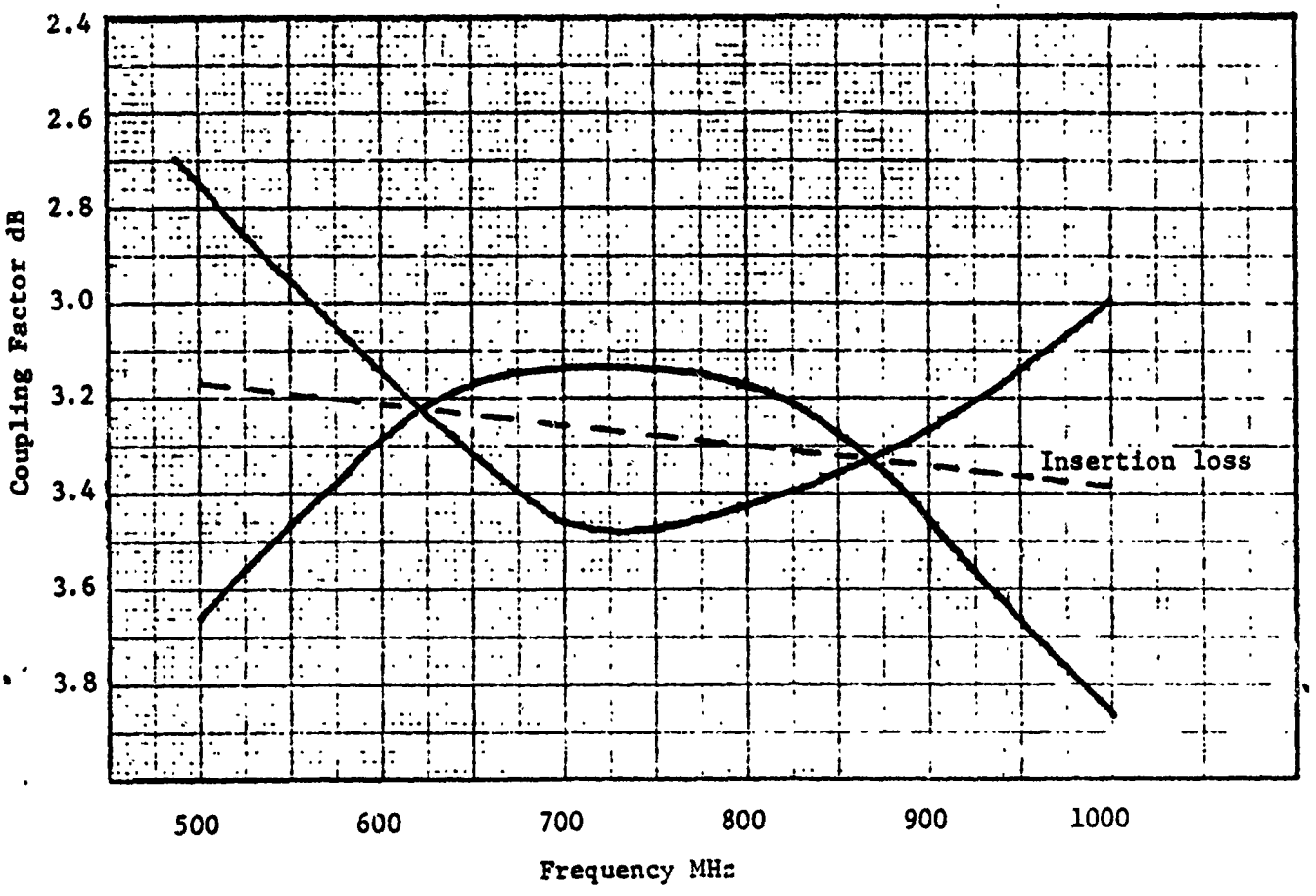


Figure 21. Performance of a Coupler Bonded with Two 1.0 Mil Bond Wires.

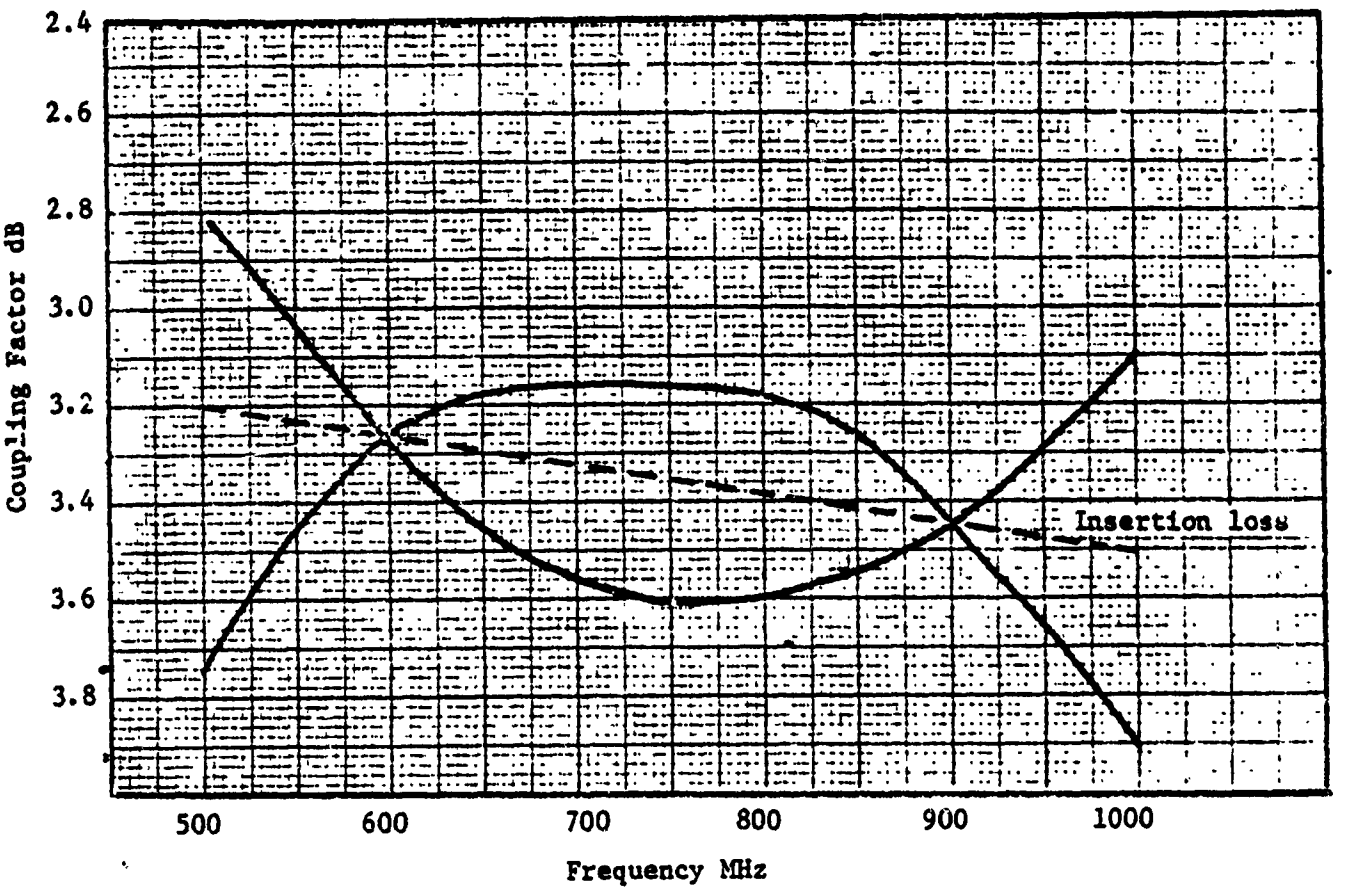


Figure 22. Performance of a Coupler Bonded With Three 1.0 Mil Bond Wires.

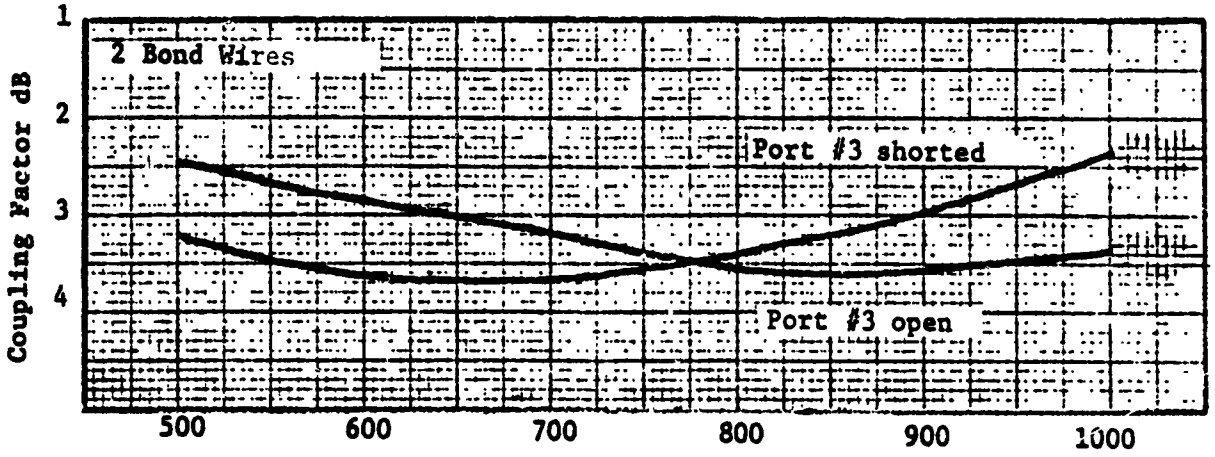


Figure 23. Port 4 Coupling Factor with VSWR on Port 3.

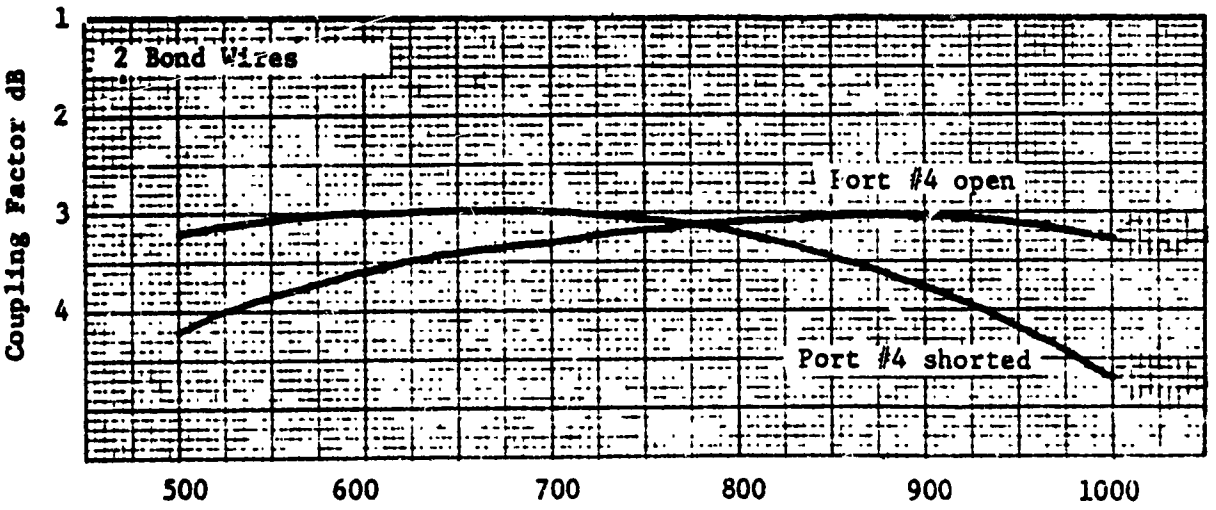


Figure 24. Port 3 Coupling Factor with VSWR on Port 4.

This thickness produces a line width at the top of the plating which was approximately 0.2 mils wider than the line width on the mask set. As the photoresist thickness cannot easily be made thicker than about 7 microns, the plating thickness must not be greater than 7 microns or the line width will increase drastically due to plated material being deposited over the edge of the photoresist, producing over-coupling.

Examination of Figures 21 and 22 indicates that the coupler is too long as the curves are centered in the 725 MHz to 750 MHz region, producing excessive coupling split at 1000 MHz. To correct this situation, the coupler length was to be reduced by a factor of 775/725 to move the curves upwards in frequency by about 50 MHz. Thus, the curves will be more centered in the 600 MHz to 1000 MHz frequency range. The insertion loss should be reduced slightly as a result of the shortening of the coupler. The length change was incorporated before fabricating the quadrature combined engineering samples. The apparent change in coupling as a function of the number of bond wires should be noted. As the data in Figures 21 and 22 was obtained from different couplers, the results are not conclusive.

The impedance measured over the 500 MHz to 1100 MHz frequency range is shown in Table I. These measurements are undoubtedly influenced by the impedance discontinuities at the connector to substrate interface. Again performance of the coupler, when used to combine the amplifiers, was expected to be somewhat better than indicated by these measurements due to the reduction of the number of connectors in the signal path.

The data shown in Figures 23 and 24 show that the couplers have isolation between the output ports.

TABLE I. PORT 1 IMPEDANCE AND VSWR VS FREQUENCY.

f(MHz)	R_{IN}	X_{IN}	VSWR
500	50	+2.5	1.05
600	50	+3.0	1.06
700	48	+2.0	1.06
800	46	+4.0	1.12
900	47	+5.0	1.07
1000	46	+4.0	1.12
1100	43	+3.0	1.15

The measurements show that a useful coupler has been produced. Allowances of 0.4 dB for maximum insertion loss and $\pm$ 0.2 dB for coupling split appear reasonable when the coupler is shortened. At a maximum output power per individual amplifier stage of 18.0 watts, the module will produce 31.4 watts of output power.

The next batch of quadrature couplers were favricated on rough surfaced alumina. The length of the coupler was not shortened so that a direct comparison could be made. These couplers exhibited performance similar to the polished substrate couplers in all respects. Figures 25 through 28 show the insertion loss and coupling characteristics of the four couplers. Figures 29 through 32 illustrate the isolation characteristics of the couplers. It should be pointed out that coupler number 4 had a short across all of the interdigitated lines due to a photoresist flaw. The short was removed by scribing the spaces between the lines with a diamond scribe. All of the conductive material may not have been removed. Therefore, the poor isolation exhibited by this coupler shown in Figure 32 is not representative of the performance expected from properly processed substrates. Table II shows the impedance data measured at the three prime ports of the four couplers. Table III shows the measured loss for a pair of couplers connected back-to-back.

In an effort to reduce the insertion loss of the couplers, two couplers were plated to an additional three microns of gold thickness. As this plating was done after the coupler completed fabrication, the line spacing was reduced by six microns thus increasing the coupling split. The increased VSWR exhibited by the plated-up couplers (Tables IV and V) tends to indicate that the line widths on the standard processed couplers are too wide. This was confirmed optically and the problem was traced to the light source collimation used for exposure of the photoresist. The performance of the plated-up couplers is shown in Figures 33 through 36. It should be noted that although

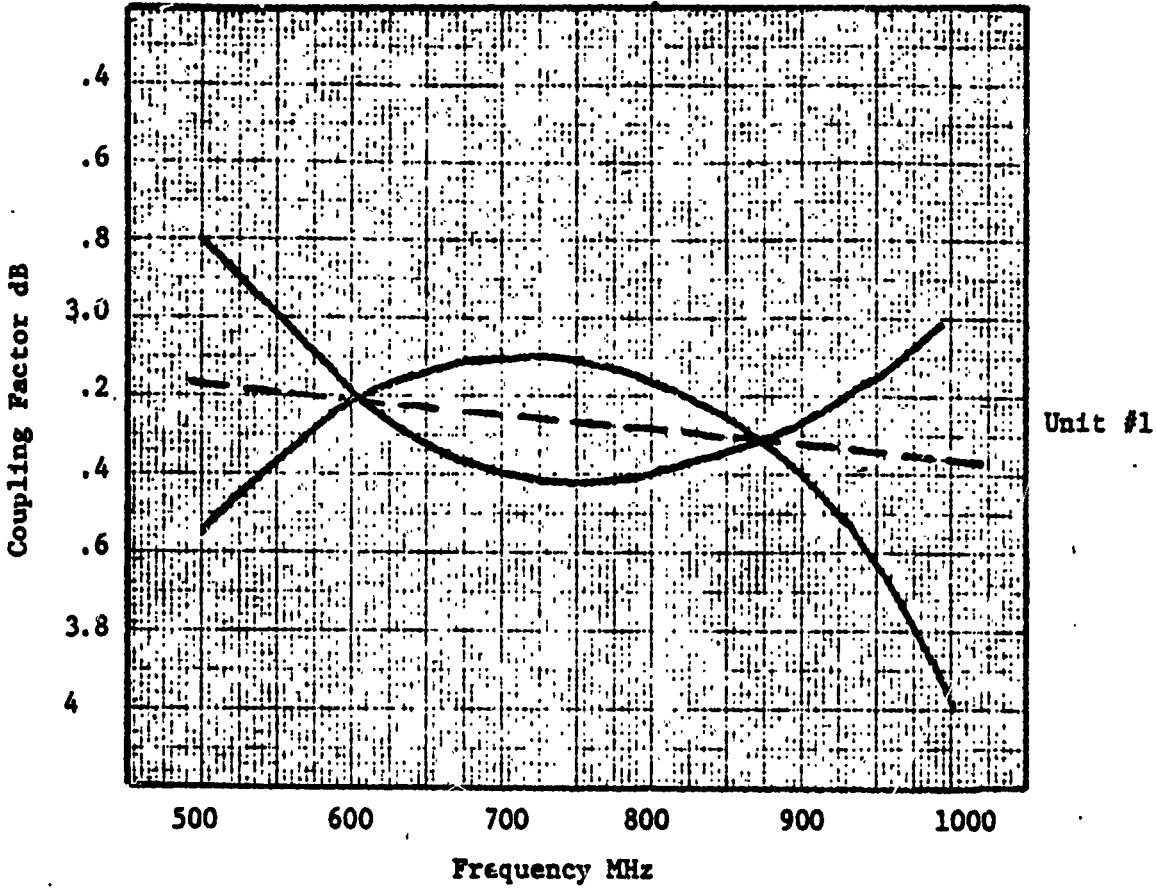


Figure 25. Power Split Coupler #1.

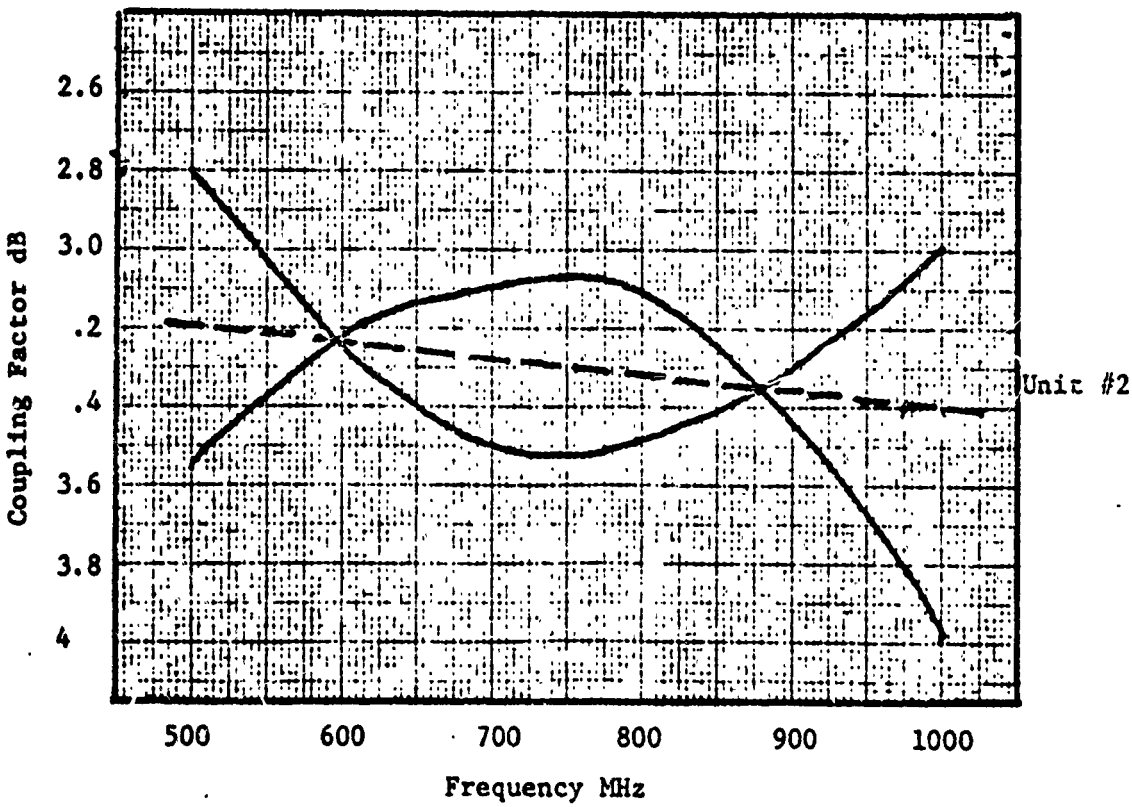


Figure 26. Power Split Coupler #2.

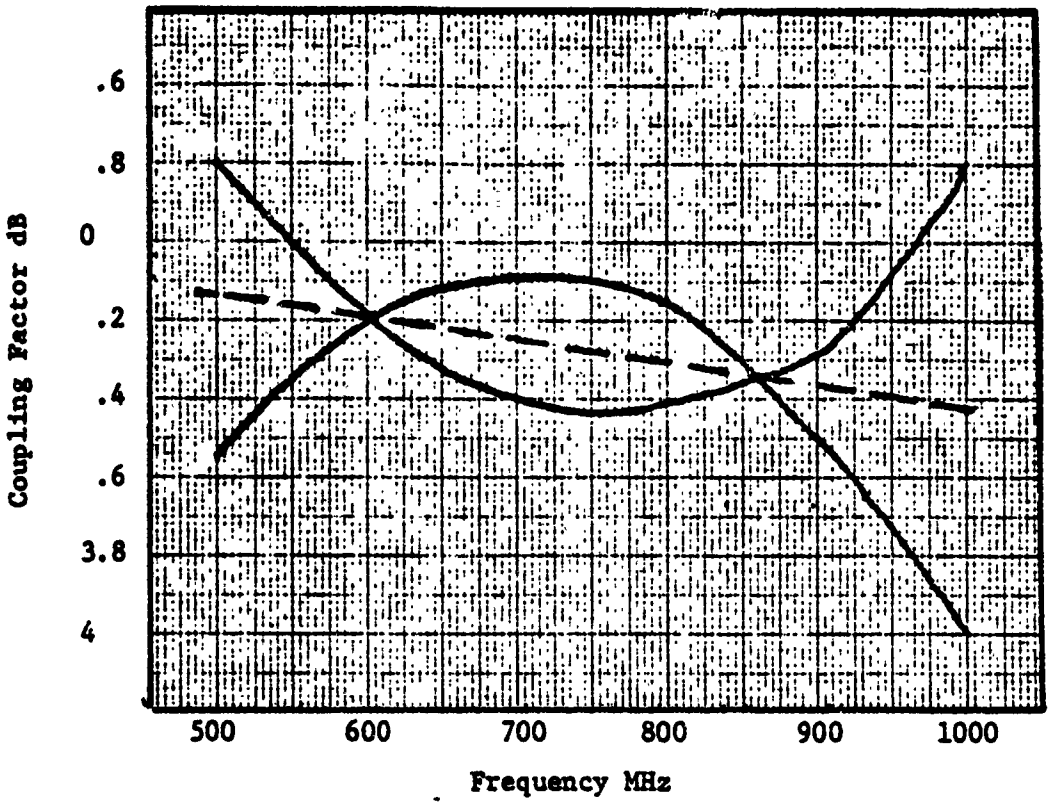


Figure 27. Power Split Coupler #3.

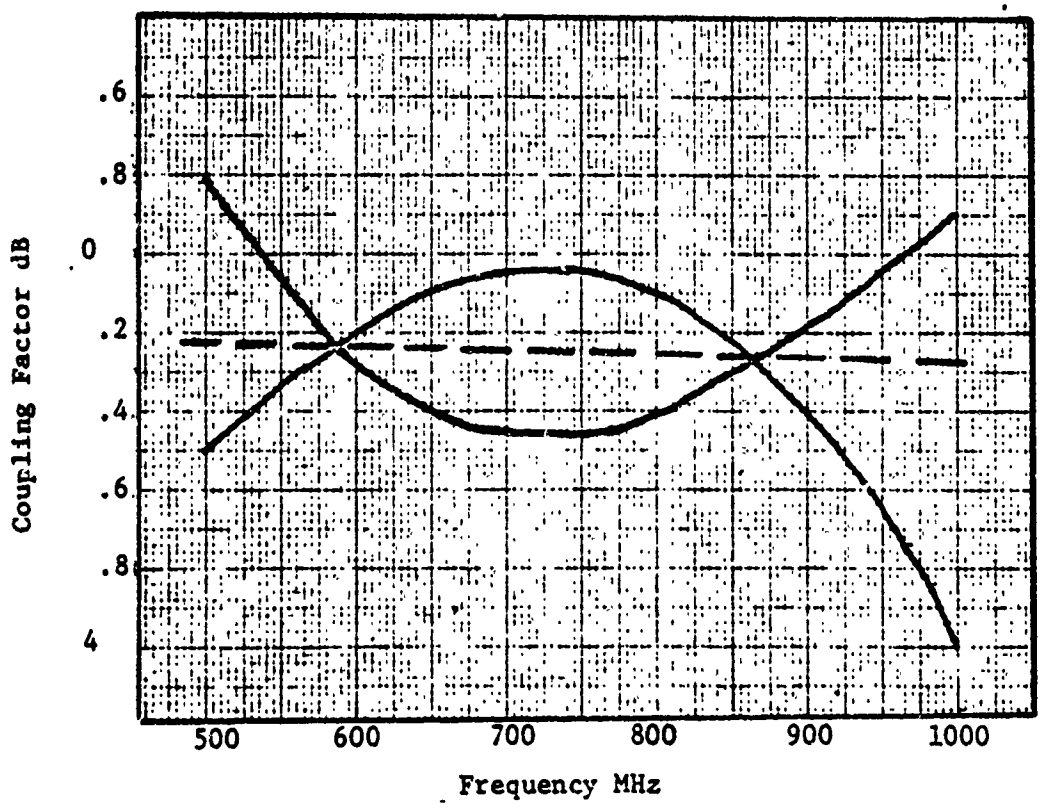


Figure 28. Power Split Coupler #4.

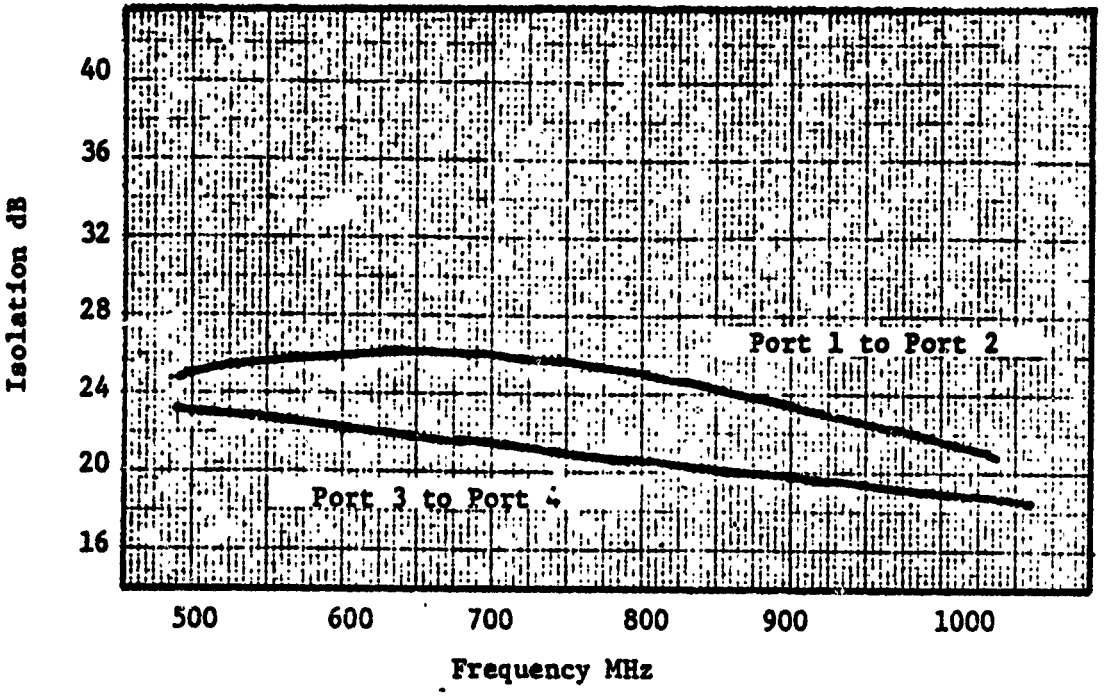


Figure 29. Coupler #1 Isolation.

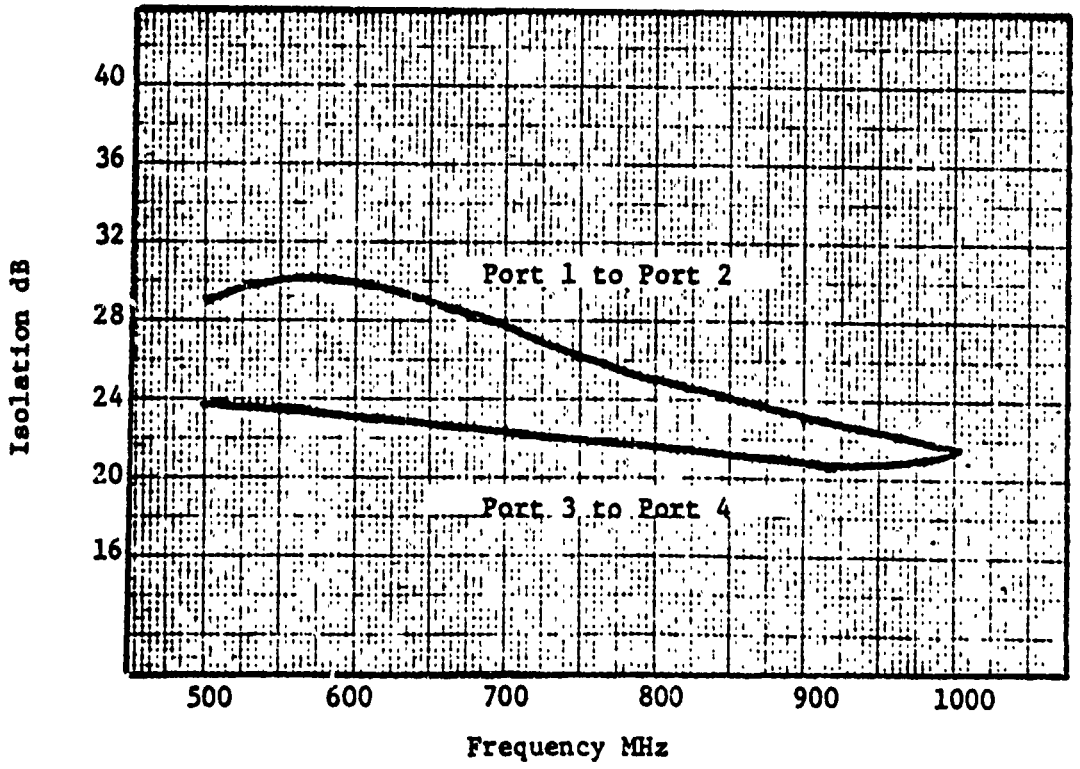


Figure 30. Coupler #2 Isolation.

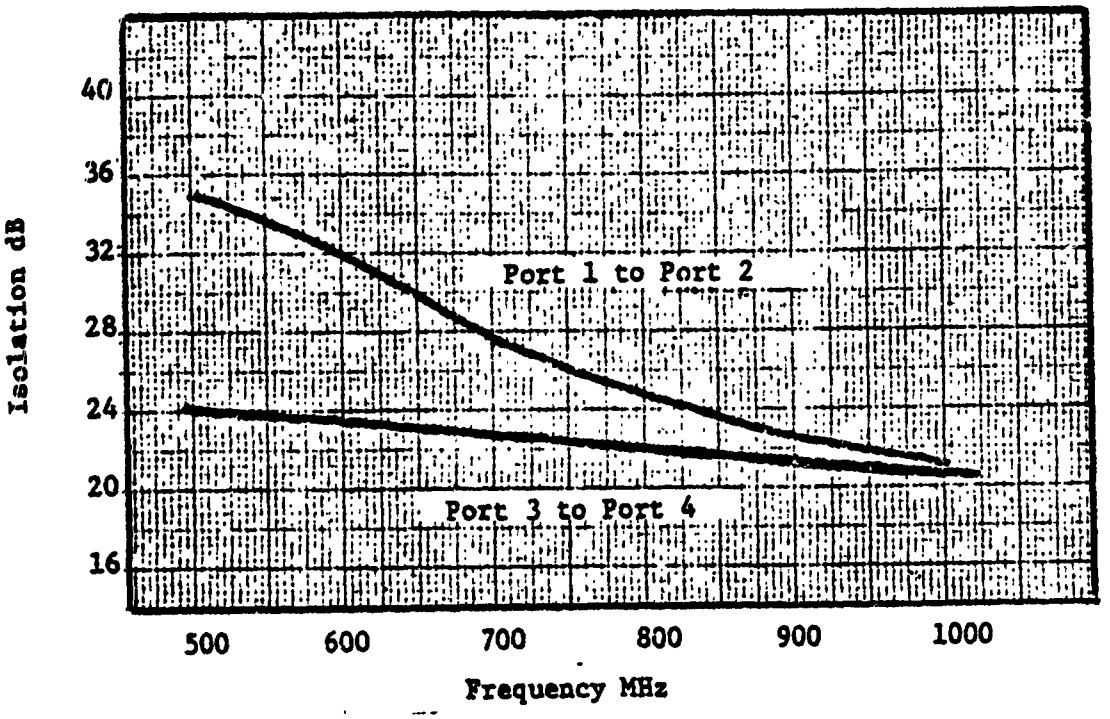


Figure 31. Coupler #3 Isolation.

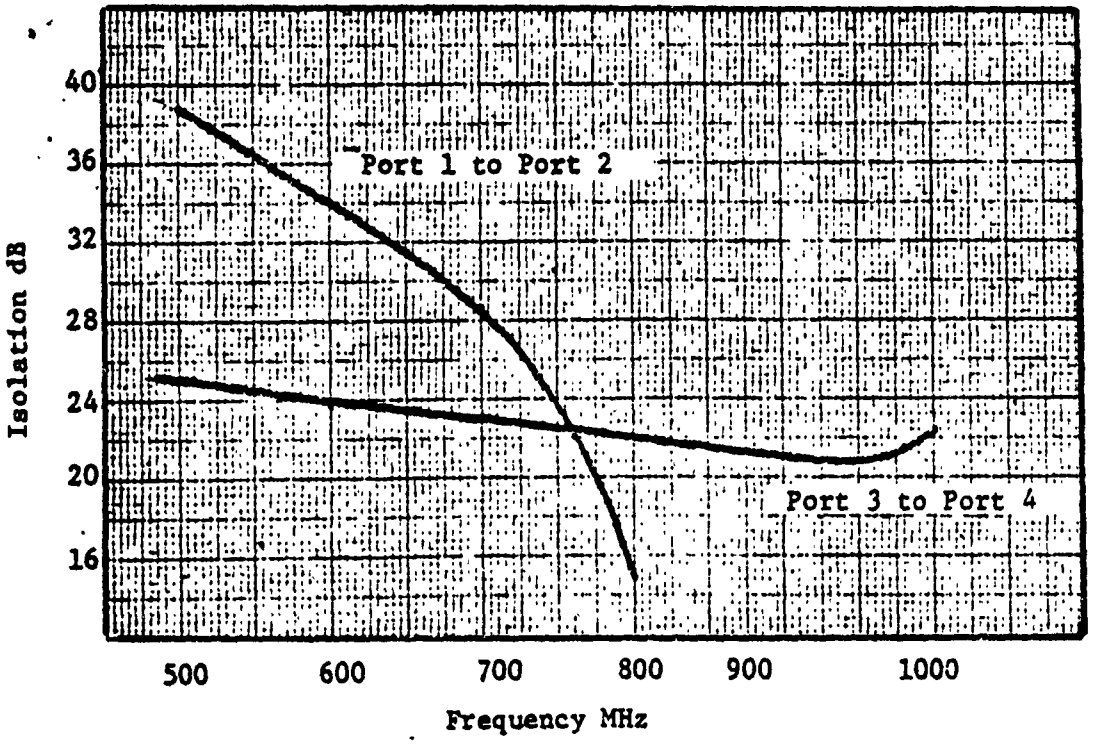


Figure 32. Coupler #4 Isolation.

TABLE II. COUPLERS #1, #2, #3, and #4 IMPEDANCE DATA.

f(MHz)	Port 1	Port 3	Port 4	
500	45.5 - j4.5	44.5 - j2.5	47 - j3.5	COUPLER #1
600	46.5 - j4.5	45.5 - j2.5	47.5 - j4	
700	45.5 - j3	44.5 - j0	47 - j3	
800	42.5 - j3	42 - j0	43.5 - j2.5	
900	40 - j4	40.5 - j1	42 - j2.5	
1000	40 - j3.5	41.5 - j0	42.5 - j2.5	
500	46.5 - j3.5	44 - j3	46.5 - j5	COUPLER #2
600	47.5 - j3.5	45.5 - j2.5	47.5 - j5.5	
700	46.5 - j2	45 - j.5	45.5 - j4.5	
800	43 - j2	42.5 - j0	42 - j4.5	
900	41.5 - j3	41.5 - j0	40 - j4.5	
1000	41.5 - j2.5	42.5 - j0	40 - j3.5	
500	46.5 - j2	44 - j2.5	46.5 - j5	COUPLER #3
600	48 - j2	45 - j4	47 - j5.5	
700	47.5 - j1	45 - j0	46 - j5	
800	44 - j1.5	42.5 - j0	42 - j5	
900	43 - j2	42 - j0	40 - j5.5	
1000	43.4 - j2	43.5 - j0	39.5 - j5	
500	47 - j3	45 - j3	47 - j3.5	COUPLER #4
600	47.5 - j3	46 - j2.5	48 - j4	
700	46.5 - j2	45 - j0	47.5 - j3	
800	43.5 - j2	42.5 - j0	43.5 - j3	
900	41.5 - j2.5	41.5 - j0	42 - j3	
1000	41.5 - j2.5	42 - j0	42 - j3	

TABLE III. INSERTION LOSS: COUPLERS 2 AND 3 BACK-TO-BACK.

f(MHz)	Loss
500	- 0.35 dB
600	- 0.40 dB
700	- 0.40 dB
800	- 0.50 dB
900	- 0.65 dB
1000	- 0.90 dB

TABLE IV. PLATED UP COUPLER #1 IMPEDANCE DATA.

f(MHz)	Port 1	Port 3	Port 4
500	47 - j5.5	42 - j4	44 - j2.5
600	48 - j5.5	42.5 - j5.5	45.5 - j4.5
700	44 - j6.5	44 - j4.5	47.5 - j4
800	41.5 - j8.5	41 - j3	44 - j3
900	41 - j10	37 - j4	40.5 - j5
1000	41 - j10	37.5 - j5	40.5 - j7

TABLE V. PLATED UP COUPLER #2 IMPEDANCE DATA.

f(MHz)	Port 1	Port 3	Port 4
500	44 - j5.5	43 - j5.5	44 - j2
600	44.5 - j8.5	42.5 - j7.5	46.5 - j4
700	44.5 - j8	44 - j6.5	48.5 - j3.5
800	43 - j7	40.5 - j4.5	46 - j3
900	39 - j8.5	36.5 - j5	42 - j5
1000	38.5 - j10	36.5 - j5.5	42.5 - j8

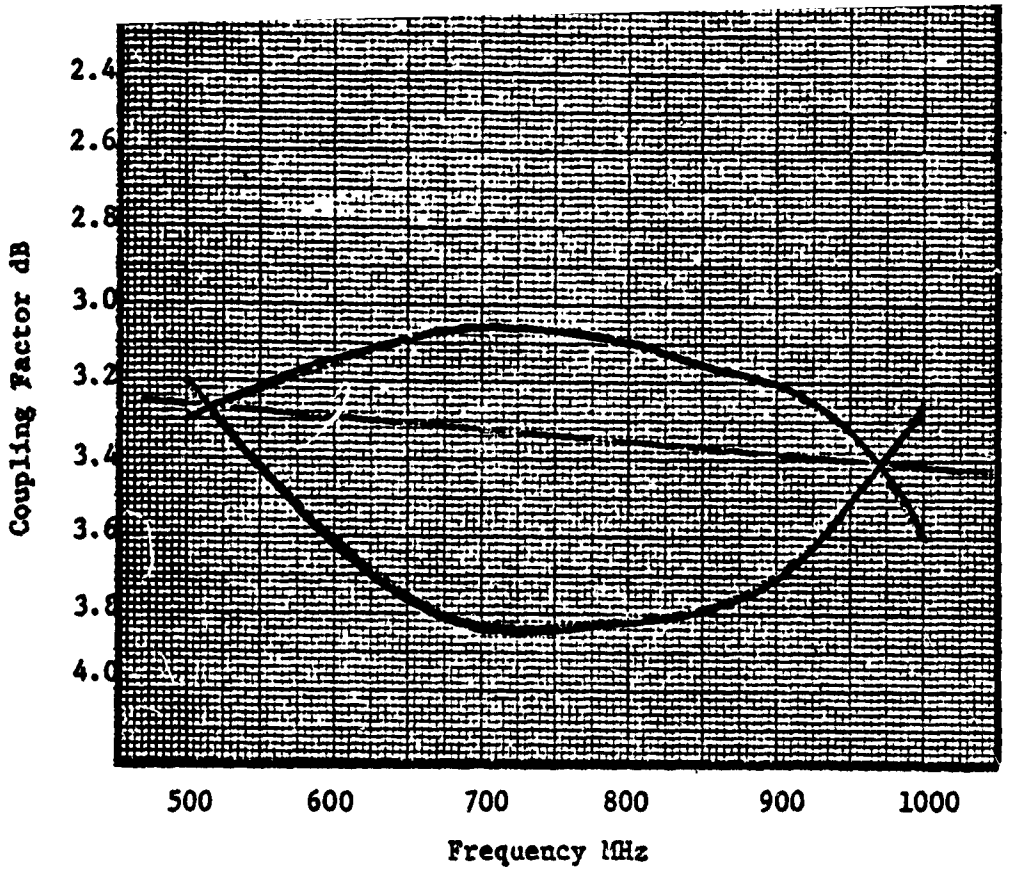


Figure 33. Power Split Plated Up Coupler #1.

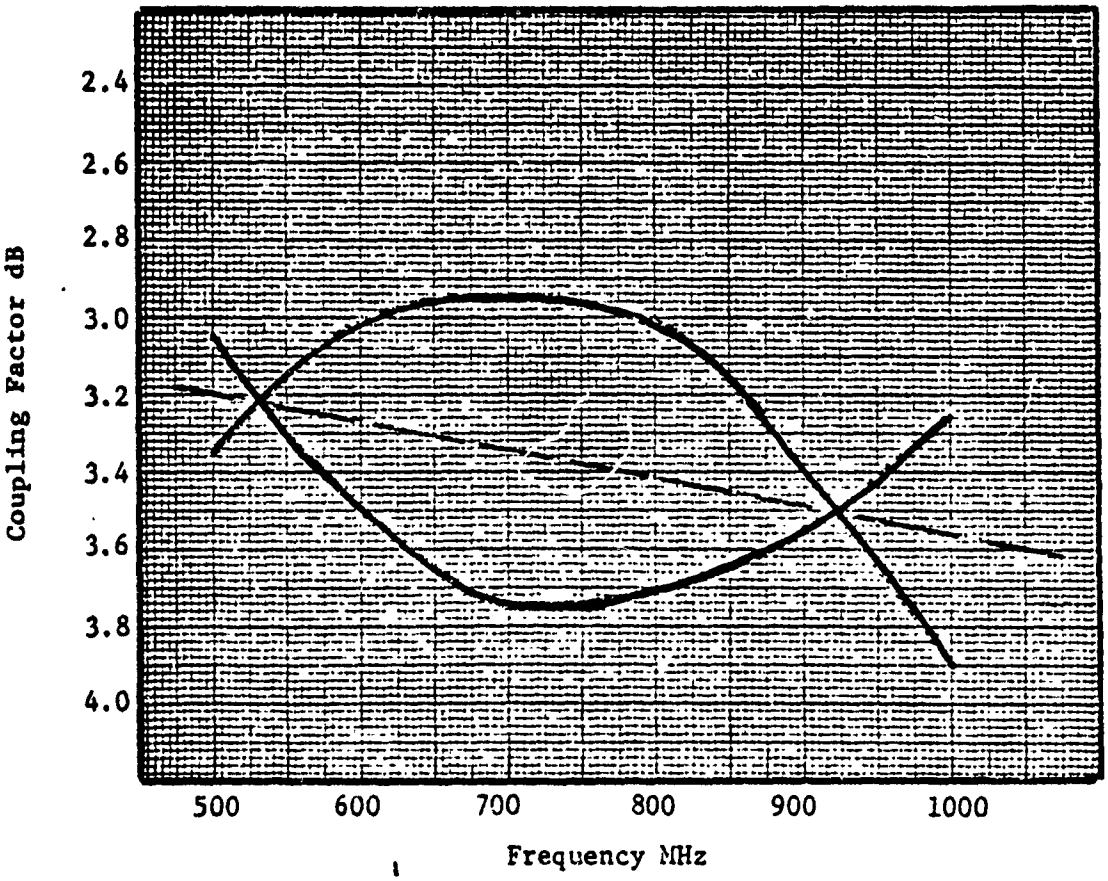


Figure 34. Power Split Plated Up Coupler #2.

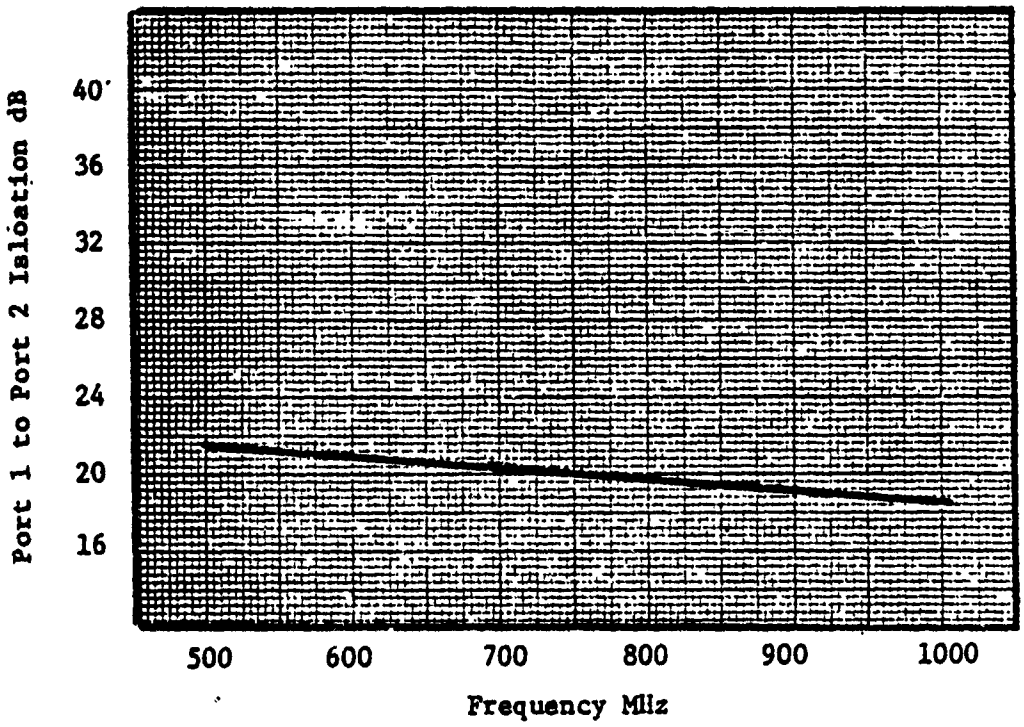


Figure 35. Isolation Plated Up Coupler #1.

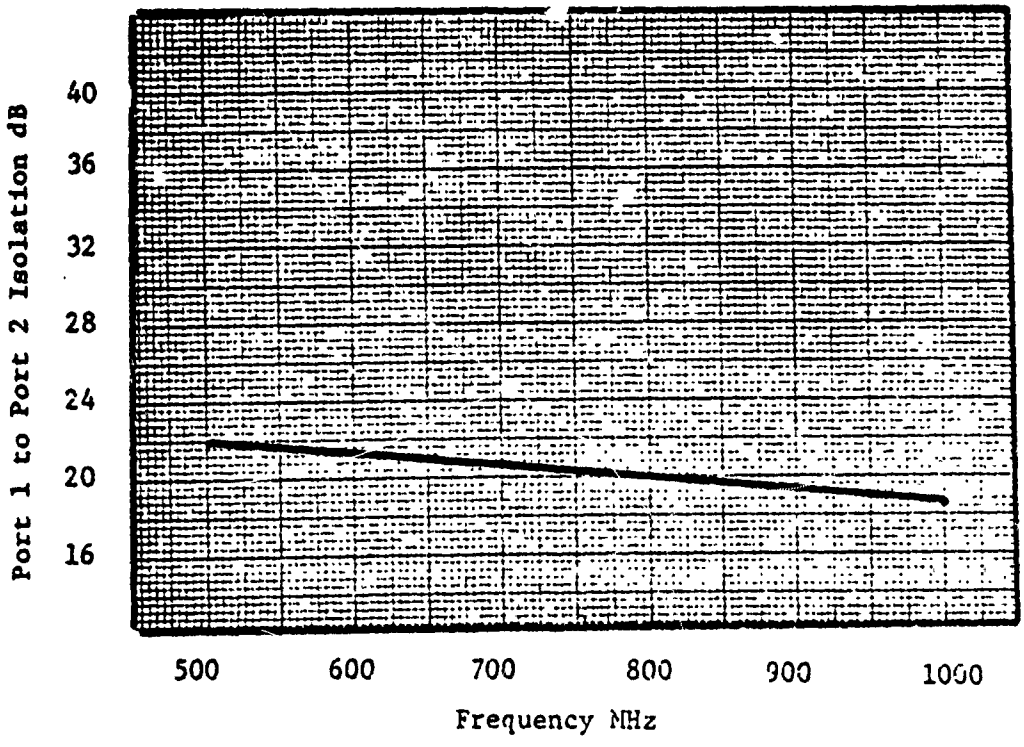


Figure 36. Isolation Plated Up Coupler #2.

the insertion is about the same as the standard couplers, an additional 0.06 dB transmission loss has been introduced due to the increased VSWR of the plated-up couplers. The additional loss exhibited by the back-to-back couplers, shown in Table VI has been attributed to phase error in the plated-up couplers.

The measurements on the six couplers show that the interdigitated quadrature couplers can be produced with a high degree of consistency. The couplers are slightly long for adequate performance at the high end of the frequency range. Steps were taken to correct the coupler length. All other parameters indicate that the coupler was adequate for completion of the contract effort.

2.2.5 Hybrid Mask and Exposure Problems

Several mask related problems were discovered during the course of this contract. The mask tolerances were held to less than 0.1 mil which appears to be near the limit of practicality. This was accomplished by making the initial mask layout at 20 times size. A pair of half sized reproductions (10X) were then made for integration with the remainder of the artwork. A 10X reduction provided the working mask. Maintaining the 0.1 mil tolerance on several masks was a slight but not insurmountable problem.

Many factors affect the gap spacing and line widths of the finished coupler. Control of these factors required that:

A. The photoresist thickness be controlled at 7 microns by interferometer measurements.

B. Exposure be controlled by light intensity measurements, collimation angle measurements and accurate exposure times.

C. Photoresist development time and temperature be controlled.

D. Plating thickness be monitored with Beta backscattering measurements.

E. A double ultrasonic etch be used to insure complete

TABLE VI. INSERTION LOSS: PLATED-UP COUPLERS 1 AND 2 BACK-TO-BACK.

f(MHz)	Loss
500	- 0.5 dB
600	- 0.45 dB
700	- 0.5 dB
800	- 0.6 dB
900	- 0.8 dB
1000	- 1.15 dB

opening of the coupler gaps.

When all of these controls were instituted it was possible to maintain a $\pm$ 0.15 mil tolerance on finished couplers. This tolerance was adequate for production of batch processed amplifiers. Comparison of Figures 33 and 34 with Figures 25 and 26 show the effects of varying the gap width by 0.24 mils.

The loss in the couplers was maintained below 0.4 dB by plating 6 to 7 microns of gold on the substrates. This plating thickness can only be reliably achieved if the photoresist used for definition is at least that thick. The exposure required for complete photoresist removal must be totally blocked by the dark areas of the mask. Therefore, the density of the opaque areas of the mask must be high enough to prevent partial exposure. This denisty was not achieved by the initial mask supplier but was by the successive vendor.

As fired alumina substrates are not flat, some warpage is present in each substrate. Thus, the mask cannot be in intimate contact with the substrate at all points. As a result, if the light source if not perfectly collimated, varying coupler aspect ratios are produced. It was necessary to use a light source collimated to less than a five degree half-angle to fabricate uniform interdigitated couplers.

2.3 DIFFERENCE PORT TERMINATION

2.3.1 Design Criterion

The performance of a quadrature coupler is greatly influenced by the termination connected to the difference port. Full performance is obtained only when the termination presents a perfect match for the unbalance power. Batch processing requirements imposed on the contract made an integrated resistor highly desirable because no installation or interconnection is required. Previous efforts to produce a high frequency, high power termination had been unsucessful due to the physical strays associated with large resistive areas on the substrate. A termination was designed to circumvent these strays.

The design concept chosen was to construct relatively small "tee" pads that each dissipate a small amount of power and then cascade a large number of these pads to provide a large power handling capability. Figure 37 is a schematic diagram of the load.

The termination was designed so that the series resistors (R1A, R1C . . . . . R12A, R12C) were one continuous lossy microstrip transmission line. The shunt resistors R1B through R12B were also microstrip transmission lines. The end of the string of pads is then terminated in a small 50 ohm load resistor.

Figure 37. Dummy Load Schematic Diagram.

Any strays in the terminating resistor are insignificant in their effect on the input VSWR of the pad because they are masked by the return loss of the attenuators.

The physical design was heavily influenced by the standard sputtering processes available. The base metals available were nichrome at 160 ohms per square. Sputtered gold was also available at 1.0 ohms per square. The other factor influencing the physical design was resistor size.

Transmission line theory states that for a lossy line, frequency independence is obtained when $R/L = G/C$ or $(R/G = L/C)$. Where R is the resistance per unit length, L is the inductance per unit length, G is the conductance per unit length, and C is the capacitance per unit length. When this condition exists, then $Zo = Ro = (L/C)^{1/2}$. Where Zo is the characteristic impedance of the line and Ro is the resistive part of Zo. The attenuation constant $\alpha = \frac{R}{Ro}$ where $\alpha = 0.1151 \times$ (Loss in dB per unit length).

As the termination was being designed for 25 mil thick alumina on which a 50 ohm transmission line is 24 mils wide, the necessary

information is determined and the design can be initiated. Assuming a thin film gold series resistor at 1.0 ohms per square, then: R = 1.0/24 = .041 ohms. And $1/G = Zo^2/R = 2500/.041 = 61{,}000$ ohms; the length of this resistor is 61,000/160Ω/□=381 mils long which exceeds the space allocation for the termination. This process was iterated until a value of 542 ohms was obtained for the shunt resistor. This value is produced by a transmission line 110 mils long and 32.5 mils wide which does fit in the allocated space. The series resistor value now becomes $(GZo^2) = 2500/542 = 4.6$ ohm and the size of this resistor is 4.6Ω/1Ω/□ = 4.6 squares which is $(L = \square_s \times W) = 4.6 \times 24 = 110$ mils long. The attenuation provided by the s tee attenuator is $\alpha = 4.6/50 = .092$ nepers or 0.8 dB. Figure 38 shows the physical layout of one tee attenuator. Twelve of these attenuators are cascaded producing 9.6 dB attenuation. The last attenuator is terminated in a 50 ohm resistor.

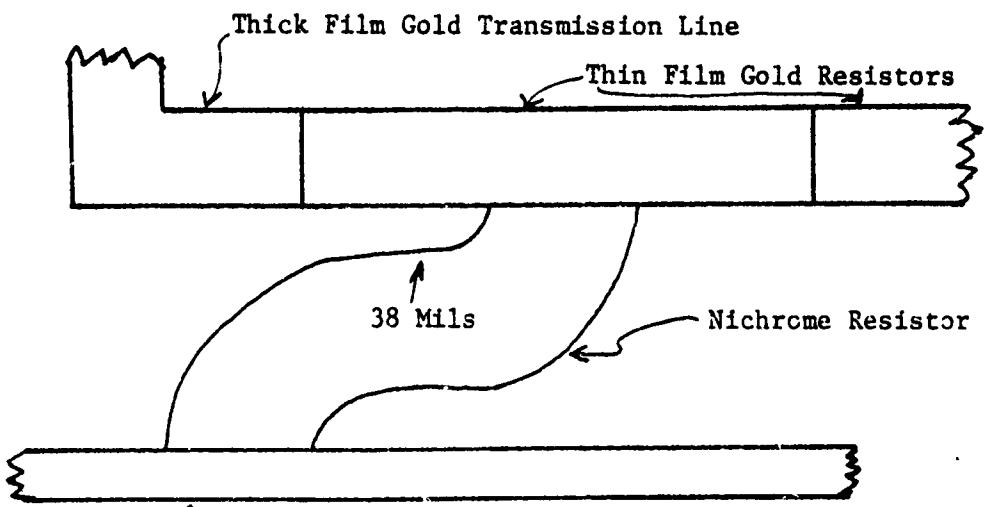


Figure 38. Tee Attenuator Layout.

Past experience with these types of resistors has proven that 400 watts per square is a very conservative rating for dissipation. Because the power applied to the load is attenuated by each sucessive attenuator, the first attenuator is subjected to the highest dissipation. Actually the first half of the series resistor has the highest dissipation of all. The power rating of this resistor is $(400W/in^2)$ (L) (W) = 400 x .055 x .024 = .528 watts. Similarly the power rating of the shunt resistor is 400 x .110 x .032 = 1.408 watts. As the power dissipated in the first half of the series, resistor is $P = I^2R$ or $I = (P/R)^{1/2}$ the allowable input current is $(.528/2.3)^{1/2}$ = .479 amps. and the allowable input power to the 50 ohm pad is $P_{in} = I^2R_o = (.479)^2$ x 50 = 11.5 watts. This input power produces a voltage across the shunt resistor of $E = (PR_o)^{1/2} - IR = (11.5 \times 50)^{1/2} - .479 \times 2.3 = 22.88$ volts and the dissipation in the shunt resistor is $P = E^2/R = (22.88)^2/542 = .965$ watts which is less than the allowable 1.408 watts.

During a later mask change the pad was redesigned for equal power dissipation in all the attenuators. Schematically this pad was idential to the previous design (Figure 37). In this design the area of each pad was adjusted by progressively making the series transmission line narrower and shorter so that the watts per square inch were held constant.

Assuming that a 30 watt termination can be fit into the existing space, the required power dissipation per resistor can be calculated.

$E = (PR)^{1/2}$ $\qquad$ $I = E/R$

$E = (30 \times 50)^{1/2}$ $\qquad$ $I = 38.75/50$

$E = 38.73V$ $\qquad$ $I = .774A$

The first series resistor in the attenuator is 2.3 ohms, therefore, 2.3 x .774 = 1.78 volts is dropped across this resistor. The first shunt resistor (R1A) has 38.73 - 1.78 = 36.95 volts across it producing a current flow of 36.95/542 = 0.068A. The current flowing

in both the second and third series resistors is 0.774 - .068 = .706A. Continuing this process:

	CURRENT	VOLTAGE DROP	OUTPUT VOLTAGE	OUTPUT CURRENT
R1A	0.774A	1.78	36.95	
R1B	0.068			0.706
R1C R2A	0.706	3.25	33.70	
R2B	0.062			0.644
R2C R3A	0.644	2.96	30.74	
R3B	0.057			0.587
R3C R4A	0.587	2.70	28.04	
R4B	0.052			0.535
R4C R5A	0.535	2.46	25.58	
R5B	0.047			0.488
R5C R6A	0.488	2.24	23.34	
R6B	0.043			0.445
R6C R7A	0.445	2.05	21.29	
R7B	0.039			0.406
R7B R8A	0.406	1.86	19.42	
R8B	0.036			0.370
R8C R9A	0.370	1.70	17.72	
R9B	0.033			0.337
R9C R10A	0.337	1.55	16.17	
R10B	0.030			0.307
R10C R11A	0.307	1.41	14.75	
R11B	0.027			0.280
R11C R12A	0.280	1.29	13.46	
R12B	0.024			0.255
R12C	0.255	0.59	13.40	

This information is used to calculate dissipation area width and length. 0.6 ohms per square will be used for series resistors and 160 ohms per square will be used for shunt resistors.

$$\text{Pd series resistor} = I^2R$$

$$\text{Pd shunt resistor} = E^2/R$$

$$\text{Area} = Pd/400\ \ln^2$$

$$\text{Number of squares} = R/\text{ohms per square}$$

$$L/W = \text{number of squares}$$

$$W = \left(A \cdot \frac{W}{L}\right)^{1/2} \qquad W^2 = A \cdot \frac{W}{L} \qquad W = \frac{A}{L} \text{ or } L = \frac{A}{W}$$

RESISTOR	P_{DISS}	AREA	W	L	SCALED W	SCALED L
R1A	1.38W	3450	30	115	25	95.8
R1B	2.52W	6300	43.1	146	35.9	121.7
R1C R2A	2.30W	5750	27.4	210	22.8	175
R2B	2.09W	5225	39.3	133	32.7	110.8
R2C R3A	1.91W	4775	24.9	191.8	20.7	159.8
R3B	1.74W	4350	35.8	121.4	29.8	101.2
R3C R4A	1.59W	3976	22.8	174.4	19.0	145.3
R4B	1.45W	3625	32.7	110.8	27.2	92.3
R4C R5A	1.36W	3400	21.0	161.4	17.5	134.5
R5B	1.21W	3025	29.9	101.2	24.9	84.3
R5C R6A	1.09W	2725	18.8	144.5	15.7	120.4
R6B	1.00W	2500	27.2	92.0	22.7	76.7
R6C R7A	.906W	2265	17.2	131.8	14.3	109.8
R7B	.837W	2093	24.8	84.2	20.7	70.2
R7B R8A	.755W	1888	15.7	120.3	13.1	100.2
R8B	.697W	1743	22.7	76.8	18.9	64.0
R8C R9A	.626W	1565	14.3	109.5	11.9	91.2
R9B	.58W	1450	20.7	70.1	17.2	58.4
R9C R10A	.519W	1298	13.0	99.8	10.8	83.2
R10B	.483W	1208	18.9	64.0	15.7	53.3
R10C R11A	.431	1078	11.9	90.9	9.90	75.7
R11B	.403	1008	17.2	58.4	14.3	48.7
R11C R12A	.358	895	10.8	82.8	9.00	69.0
R12B	.336	840	15.7	53.3	13.1	44.4
R12C	.148	370	9.82	37.7	8.20	31.5

Total Length = 1679.9 mils.

Since only 1400 mils of length was available the series resistors are 20 percent too long. Therefore, all resistor sizes were scaled down by 20 percent producing a 25 watt termination. The series

resistors were laid out to the calculated taper but the shunt resistors were not individually tapered. A 112 mil long, 32 mil wide resistor was used for the first seven attenuators. The last five attenuators used 60 mil long, 17 mil wide resistors due to space problems. This reduction in area further derates the allowable input power to 17 watts at 400 watts per square inch. This is still a significant improvement over the non uniform dissipation design.

2.3.2 Termination Adjustment Techniques

Initially the pad was designed so that adjustment could be done by etching the resistive material to increase the resistance to the desired values. Attempts to etch the nichrome material failed because the etching rate was unpredictable. The thin film gold etch was predictable but visible non-uniformity was produced. The later designed equal power distribution, termination solved both of these problems. The thin film gold resistor was sputtered to 0.6 ohms per square and not adjusted. Cermet was used for the shunt resistors and was etched to accommodate the variations in both the series resistors and the shunt resistors. Performance characteristics were unaffected by this change. As fabrication techniques were not changed the problem solution was attributed to the design change.

2.3.3 Termination Test Results

The initial design terminations were tested for VSWR. The results are shown in Table VII.

TABLE VII. VSWR OF INITIAL DESIGN TERMINATIONS

Frequency (MHz)	VSWR	
	Unit #1	Unit #2
dc	1.03	1.08
600	1.03	1.08
700	1.04	1.10
800	1.04	1.09
900	1.04	1.08
1000	1.06	1.10
1200	1.12	
1500	1.22	
2000	1.30	
3000	1.32	
4000	1.38	

The equal power dissipation design was also tested for VSWR over the 600 to 1000 MHz frequency range. The results are shown in Table VIII.

TABLE VIII. VSWR OF EQUAL POWER DISSIPATION TERMINATION.

Frequency (MHz)	VSWR
600	1.05
700	1.08
800	1.10
900	1.12
1000	1.14

The equal power dissipation load shows some slight degradation in performance but the VSWR is very acceptable for the 600 MHz to 1000 MHz frequency range. The added power capability of the load gives lower termination stress levels when used in the contract amplifier.

2.4 CHARACTERIZATION

Characterization is the process of determining the characteristics of the transistor chip so that matching networks can be designed for maximum power transfer into and out of the chip. The procedure used is:

1. Assumption of a general model for the device based upon the best information available.
2. Design of matching networks to match the model impedances to the desired source and load impedance.
3. Fabrication of transistors and circuitry for impedance measurements.
4. Readjustment of the model for a better fit with the measured results.

This process is iterated until the desired results are obtained.

2.4.1 Characterization of the MW1 Transistor

Characterization of the transistors for the amplifier was done on both a single cell 2.5 watt transistor and an eight cell 20 watt transistor. The single cell transistor was characterized because it is easier to make accurate measurements at the higher impedance levels associated with the single cell. The eight cell impedance measurements, though not as accurate, are useful for determination of scaling factors and degradation of performance due to cell combining problems.

2.4.2 MW1 Output Characterization

The model of a microwave transistor has the general form

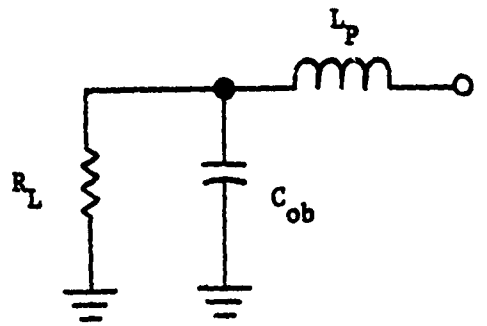
shown in Figure 39. R_L is the load impedance presented to the collector at the chip. Although it is well known that a transistor is a current generator and thus has an output impedance much greater than the load impedance impressed upon it, it is convenient to think of the transistors output impedance as the conjugate of the load impedance. The capacitor in the model is the total collector-base capacitance and consists of both a fixed and a voltage variable capacitance. L_p is the package parasitic inductance. This inductance is measured by shorting the collector pad to the ground metalization on the BEO carrier and measuring the impedance from the output lead to ground. Establishment of the load impedance (R_L) is also relatively straightforward. Assumption of sinusoidal collector voltage allows the use of the classic formula:

$$R_L = \frac{(V_{cc} - V_{ce}\ Sat)^2}{2\ P_o}$$

V_{cc} = Collector supply voltage
V_{ce} Sat = Collector emitter saturation voltage
P_O = Output power

This assumption is valid because the transistor efficiencies are in the 50 to 60 percent region. When these efficiencies are compared to the theoretical 50 percent of a class A amplifier (purely sinusoidal waveshape) one may conclude that collector waveshapes are similar. Practical experience has also demonstrated that such is the case. The determination of V_{ce} sat is difficult because it is a function of the transistor cell design and frequency. Past experience with the MW1 cell indicated that V_{ce} Sat was approximately 2.5 volts in the 600 to 1000 MHz frequency range. Therefore:

18 watt amplifier: $R_L = \frac{(28 - 2.5)^2}{2 \times 18} = 18\ \Omega$



$R_L \approx$ Collector load impedance $= \frac{V_{cc}^2}{2P_o}$

C_{ob} = Total collector to base capacitance

L_p = Package parasitic inductance

Figure 39. Device Output Equivalent Circuit.

2.5 watt amplifier: $R_L = \frac{(28 - 2.5)^2}{2 \times 2.5} = 130\ \Omega$

The determination of C_{ob} is more difficult because the collector voltage waveshape cannot be measured. The approach used for the initial estimate of C_{ob} was to measure the collector base capacitance cell at different voltages. Both eight cell and one cell transistors were measured and the data is shown in Tables IX and X. The measured capacitances are the toal of the package, the fixed MOS capacitance and the voltage variable cell capacitance. Next, the data for each type of transistor was averaged to establish a typical value. The average values are shown in Table XI.

Since a microwave transistor has an abrupt collector base junction; a 0.47 voltage exponent can be assumed if the effects of base widening are ignored. The classical equation can now be used to separate the fixed and voltage variable components of the measured capacitances.

TABLE IX. C_{ob} FOR 3 CELL PARTS.

VOLTS dc	C_{ob} #1 pf	C_{ob} #2 pf	C_{ob} #3 pf
1	27.7	27.5	27.5
1.5		24.5	25.0
2	22.9	22.8	23.1
3	20.4	20.0	20.7
4	18.7	18.4	19.3
6	16.5	16.4	17.0
8	15.1	15.0	15.6
10	14.2	14.2	14.8
15	12.9	12.9	13.7
20	12.3	12.3	12.1
24	12.0	12.0	11.4
28	11.7	11.8	11.1

TABLE X. C_{ob} FOR 1 CELL PARTS.

VOLTS dc	C_{ob} #1	C_{ob} #2
1	3.41	4.22
1.5	3.20	3.86
2	3.00	3.61
3	2.86	3.82
4	2.70	3.06
6	2.54	2.85
8	2.42	2.68
10	2.35	2.57
15	2.23	2.43
20	2.18	2.36
24	2.15	2.32
28	2.13	2.29

LE XI. COMPARISON OF C_{ob} FOR SINGLE CELL AND EIGHT CELL DEVICES.

V_{CB} VOLTS	C_V 1 cell pf (Avg)	8 x C_V 1 cell pf	C_{TOT} 8 cell pf (Avg)	DIFFERENCE pf
1	2.15	17.2	27.6	10.4
2	1.65	13.2	22.9	9.7
4	1.21	9.7	18.8	9.1
8	.88	7.0	15.2	8.2
16	.66	5.3	13.2	7.9
28	.54	4.3	11.9	7.6

$$C_V = C_{VO}\left(\frac{Vo + 0.75}{V + 0.75}\right)^{\eta}$$

C_V = capacitance at voltage V

C_{VO} = capacitance at voltage Vo

By using the 3 volt and 18 volt averaged measured capacitances for the single cell transistors and the 0.47 exponent:

$$C(18V) = C(3V)\left(\frac{3.75}{18.75}\right)^{0.47}$$

$$\frac{C(18V)}{C(3V)} = \left(\frac{3.75}{18.75}\right)^{0.47} = 0.469$$

As previously stated the measured capacitances are the sum of both fixed and variable parts

C fixed + C variable (3V) = 2.87

C fixed + C variable (18V) = 2.22

from the varicap equation:

C variable (18V) = 0.469 C variable (3V)

substituting

C fixed + C variable (3V) = 2.87

C fixed + 0.469 C variable (3V) = 2.22

0.531 C variable (3V) = 0.65

and

C variable (3V) = 1.22 pf.

or

C fixed = 2.87 - 1.22 = 1.65 pf.

The varicap equation may now be used to calculate the variable capacitance at any voltage. The calculated variable capacitances are shown in Table XI. Multiplying the calculated vaiable capacitances by eight and comparing them to the measured values for the eight cell transistors shows that about 0.7 picofarads must be subtracted from the fixed capacitance calculated for the single cell

transistor for best agreement over all voltages. This is the package capacitance and was verified by independent measurement. Now the time averaged value of C_{ob} can be calculated. If a purely sinusoidal voltage waveshape appears at the collector base junction integration may be used to establish the average value of C_{ob}. Since the sinusoid is impressed on a C collector voltage the collector voltage at any instant is:

$$E_c = V_{cc} + (V_{cc} - V_{ce}(SAT)) \sin \theta$$

as previously stated

$$V_{cc} = 28V \text{ and } V_{ce}(SAT) = 2.5V$$

therefore:

$$E_c = 28 + (25.5) \sin \theta$$

The varicap equation $CV = CVo \left(\frac{Vo + 0.75}{V + 0.75} \right)^{\eta}$ is again used to calculate the voltage variable capacitance at 10 degree increments.

θ	Vc3	$\frac{V+0.75}{28+0.75}$	$\left(\frac{V+0.75}{28.75}\right)^{0.47}$	CV
0	28.00	1.000	1.000	0.560
10	32.43	1.154	1.070	0.523
20	36.72	1.303	1.113	0.494
30	40.75	1.443	1.188	0.471
40	44.39	1.570	1.236	0.453
50	47.53	1.679	1.276	0.439
60	50.08	1.786	1.307	0.428
70	51.96	1.833	1.330	0.421
80	53.11	1.870	1.343	0.417
90	53.50	1.887	1.348	0.415
100	53.11	1.870	1.343	0.417
110	51.96	1.833	1.330	0.421
120	50.08	1.786	1.307	0.428
130	47.53	1.679	1.276	0.439
140	44.39	1.570	1.236	0.453
150	40.75	1.443	1.188	0.471
160	36.72	1.303	1.113	0.494
170	32.43	1.154	1.070	0.523
180	28.00	1.000	1.000	0.560
190	23.57	0.846	0.924	0.606
200	19.28	0.697	0.843	0.664
210	15.25	0.556	0.759	0.737
220	11.61	0.430	0.672	0.833
230	8.47	0.321	0.586	0.956
240	5.91	0.232	0.503	1.113
250	4.04	0.167	0.431	1.300
260	2.89	0.127	0.378	1.479
270	2.50	0.113	0.359	1.560
280	2.89	0.127	0.378	1.479
290	4.04	0.167	0.431	1.300
300	5.91	0.232	0.503	1.113
310	8.47	0.321	0.586	0.956
320	11.61	0.430	0.672	0.833
330	15.25	0.556	0.759	0.737
340	19.28	0.697	0.843	0.664
350	23.57	0.846	0.924	0.606

The total of the CV column is 25.763 and the average value of the voltage variable capacitance is $\frac{25.763}{36}$ 0.716 pf per cell. This gives a 5.72 pf voltage variable capacitance for an eight cell transistor. Next, the previously calculated fixed capacitance (0.95 pf x 8) is added to the time averaged value of voltage vaiable capacitance to

produce a C_{ob} value of 13.3 picofarads. Because it is known that the collector voltage waveshape is not sinusoidal due to the emitter base contact potential this calculated value of C_{ob} is higher than the true value for a non-linear case and this number must be adjusted downward by some factor. The value of C_{ob} for the single cell transistor is the sum of the voltage variable capacitance, the fixed capacitance, and the package capacitance (0.716 + 0.95 + 0.7 = 2.36 pf). Package capacitance is not included in the eight cell model because the collector impedance is much lower than the Zo of the collector pad and therefore the collector pad will behave as an inductance rather than a capacitance.

The models for both the single cell and eight cell transistors have now been determined. The next step is to trace the model from the device to the package output lead. This was accomplished through the use of an immittance chart and the output impedances are shown in Table XII.

Circuits are now required for evaluation of the transistors. Manipulation on an immittance chart of the single cell output impedances produced the circuit shown in Figure 40. This was built and adjusted to the conjugate impedances for the single cell transistor shown in Table XII through the use of a network analyzer. Inserting a transistor into the test fixture and tuning the input stub tuner at each frequency produced the performance shown in Table XIII. The low efficiency obtained at 800 and 900 MHz was expected from the discrepancy between the modeled impedances and the achievable circuit tuning impedances. Therefore, a stub tuner was inserted to correct the output impedance and individual frequency measurements were taken.

TABLE XII. OUTPUT EQUIVALENT CIRCUIT IMPEDANCES.

FREQUENCY MHz	EIGHT CELL DEVICE Z_O REAL OHMS	EIGHT CELL DEVICE Z_O IMAG OHMS	ONE CELL DEVICE Z_O REAL OHMS	ONE CELL DEVICE Z_O IMAG OHMS
550	10.7	-7.4	62.8	-63.7
600	10.0	-7.5	57.2	-63.2
650	9.3	-7.5	52.2	-62.3
700	8.6	-7.4	47.6	-61.1
750	7.8	-7.3	43.5	-59.7
800	7.2	-7.2	39.9	-58.2
850	7.0	-7.0	36.6	-56.6
900	6.4	-6.8	33.7	-55.0
950	5.9	-6.6	31.1	-53.3
1000	5.5	-6.4	28.7	-51.7
1050	5.4	-6.2	26.6	-50.1

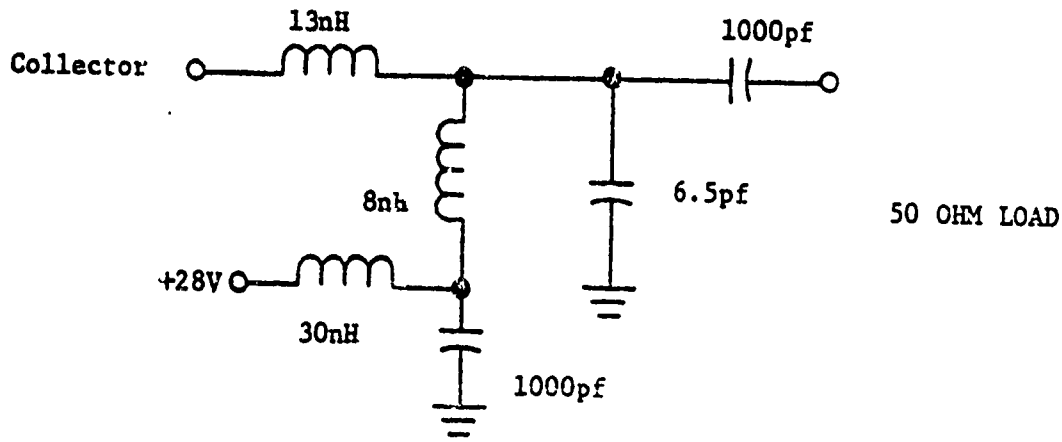


Figure 40. Output Matching Circuit Used for Testing Single Cell Devices.

TABLE XIII. BROADBAND SINGLE CELL DEVICE PERFORMANCE.

FREQ. MHz	P_{IN} WATTS	P_{OUT} WATTS	I_C mA	EFFICIENCY PER CENT
600	.26	2.5	157	57
700	.28	2.5	174	51
800	.30	2.5	187	48
900	.33	2.5	189	47
1000	.33	2.5	168	53

The performance and impedance data obtained are shown in Table XIV. When the model values for R1 and C_{ob} are adjusted for optimum fit with the measured data (circuit configuration shown in Figure 39) the real load at the collector of the device is 180 ohms and the value for C_{ob} is 2.7 pf. Calculation of the voltage swing required to produce thie value of load impedance can now be accomplished using the formula:

$$Vcc = \sqrt{R1\ 2Po} = \sqrt{180 \times 5} = 30V.$$

As this value is greater than the supply voltage an error exists. This error is probably due to a departure from the previously assumed sinusoidal collector voltage waveshape, a condition that occurs at higher efficiencies. In any event it has been shown that the single cell is capable of producing efficiencies of 55 percent or better over the 600 MHz to 1000 MHz band in a perfectly matched broadband circuit.

The circuit for evaluating the performance of the eight cell transistor was extracted from a previous design. A drawing of this circuit is shown in Figure 41. Again the circuit tuning was adjusted as closely as possible to the conjugate of the model impedances for the eight cell transistor (Table XII) by using a network analyzer. Inserting the transistor and individually tuning the input at each frequency with a stub tuner produced the performance shown in Table XV. It was impossible to improve the average efficiency or average gain by modification of the circuit. High end performance could be sacrificed for low end performance and vice versa, but overall the performance could not be improved. The low efficiency at the low end of the band was due to insufficient match provided by the stub tuner indicated by the high reflected power. Increasing the drive at 600 MHz did produce more output power and better efficiency but data was not recorded. This data indicates that the initial model was correct and further iteration is not necessary.

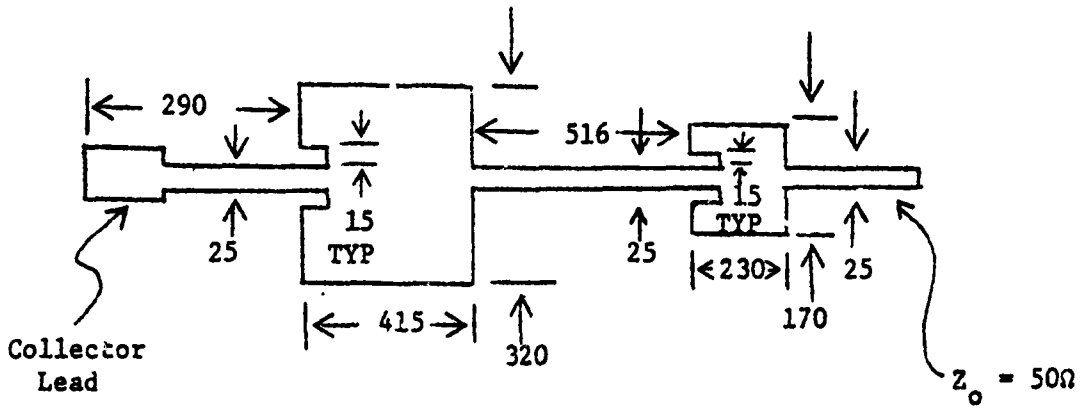
TABLE XIV. SINGLE CELL DEVICE PERFORMANCE AND IMPEDANCES OPTIMIZED AT EACH FREQUENCY.

SINGLE CELL DEVICE #1

FREQ.	P_{IN}	I_C	EFFICIENCY	CONJUGATE IMPEDANCES			
MHz	mW	mA	PER CENT	$Z_{IN}(\Omega)$ REAL	$Z_{IN}(\Omega)$ IMAG	$Z_O(\Omega)$ REAL	$Z_O(\Omega)$ IMAG
600	220	148	60	9.5	-1.5	42.5	75
700	207	140	64	7.0	-1.0	37.5	70
800	200	137	65	5.0	+1.0	25	65
900	234	144	62	5.5	+1.7	20	60
1000	226	153	58	6.0	+2.5	15	45

SINGLE CELL DEVICE #2

FREQ.	P_{IN}	I_C	EFFICIENCY	CONJUGATE IMPEDANCES			
MHz	mW	mA	PER CENT	$Z_{IN}(\Omega)$ REAL	$Z_{IN}(\Omega)$ IMAG	$Z_O(\Omega)$ REAL	$Z_O(\Omega)$ IMAG
600	230	150	59	8.0	-2.0	40.0	65
700	220	150	59	7.0	-1.0	37.5	62
800	200	157	57	6.0	0.0	35.0	60
900	200	150	59	6.0	+1.5	20.0	54
1000	220	154	58	6.0	+2.5	16.5	41



Circuit fabricated on 25 Mil Alumina.
All dimensions in Mils.
Collector dc Feed Choke is connected as close to device package as possible.

Figure 41. Output Matching Circuit Used for Testing the First Eight Cell Device.

TABLE XV. BROADBAND EIGHT CELL DEVICE PERFORMANCE.

FREQUENCY MHz	REFLECTED P_{IN} WATTS	P_O WATTS	I_C AMPS	EFFICIENCY PER CENT
600	1.13	8.4	.75	40
650	.68	14.4	1.11	46
700	.40	20.4	1.45	50
800	.24	20.8	1.52	48
900	.36	19.0	1.37	49
1000	.30	18.4	1.37	48

P_{IN} held constant at 2.0 Watts V_{cc} = 28.0V

2.4.3 MW1 Input Characterization

The input impedance of the devices was also measured by the conjugate method. That is, the device was removed from the circuit and the impedance presented to it was recorded. To determine the impedance at the emitter base junction a dummy device was fabricated by scrubbing down a gold plated metal strip in place of the transistor chip. The emitter bond wires were bonded at the exact place on the metal strip that the emitter bonding pads would be had a transistor chip been mounted in the package. The other end of the bond wire was bonded to the input lead in the normal place. The impedance of this dummy package was measured and subtracted from the conjugate impedances previously recorded to produce the impedances shown in Table XIV.

The synthesis of an equivalent circuit for the input impedance presented a particular problem. The computer network analysis and synthesis programs available when this work was done would not accommodate parallel branching in series elements. Therefore, it was necessary that the equivalent circuit generated avoided the necessity for such a network configuration even though it is known that transistor equivalent input circuits contain a parallel resistance capacitance in series with the base bulk resistance.

The MW1 single cell source impedances were measured during output characterization work. From the conjugates of the measured impedances the equivalent circuit shown in Figure 42 was synthesized. This circuit is compatible with the computer network programs and exhibits the impedance-characteristics shown in Table XVI. A Smith chart comparison of the measured input and output impedances is shown in Figure 43.

From this comparison it can be seen that the input model is as accurate as the revised output model for a single cell transistor.

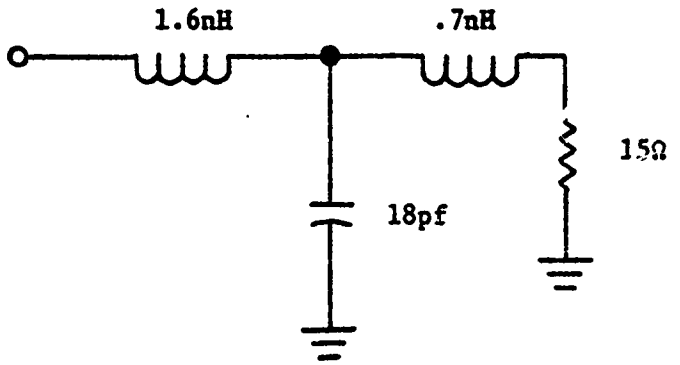


Figure 42. Single Cell Device Equivalent Input Circuit.

TABLE XVI. SINGLE CELL DEVICE EQUIVALENT INPUT CIRCUIT IMPEDANCE.

FREQUENCY MHz	Z_{IN} REAL OHMS	Z_{IN} IMAG OHMS
600	8.77	-1.63
700	7.57	-.775
800	6.50	.256
900	5.58	1.41
1000	4.79	2.63

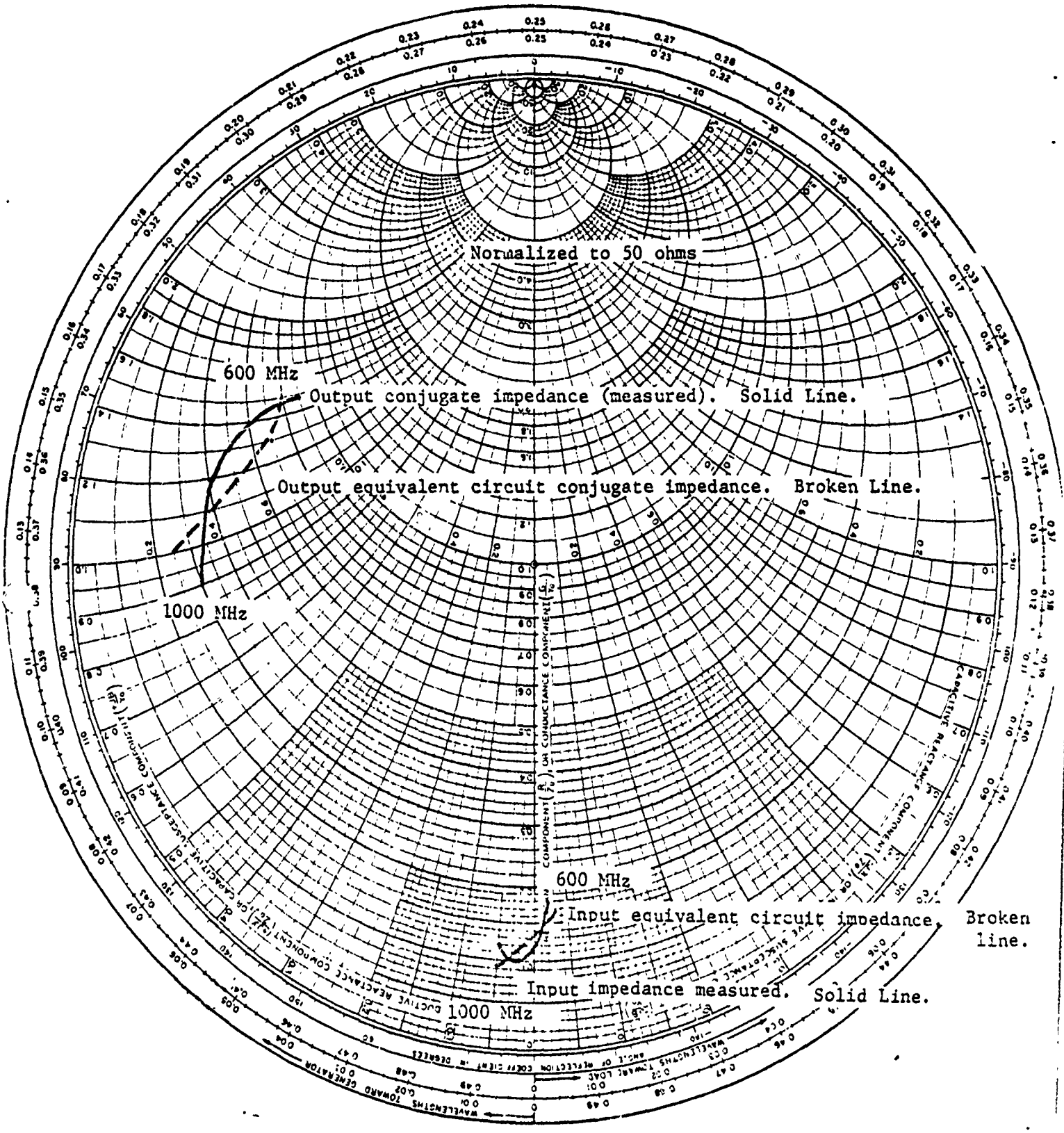


Figure 43. Comparison of the Measured Input and Output Impedances for a Single-cell Device.

The input equivalent may be scaled directly by a factor of eight to obtain the input impedance for an eight cell device.

2.4.4 Output Matching Network Design

The output matching network used for characterization of the eight cell transistor was discarded for two reasons. First, it occupied too much physical space for integration on the size substrate planned for use in the amplifier. Secondly, 180 degree couplers were still being considered and they presented a 25 ohm load to the matching network.

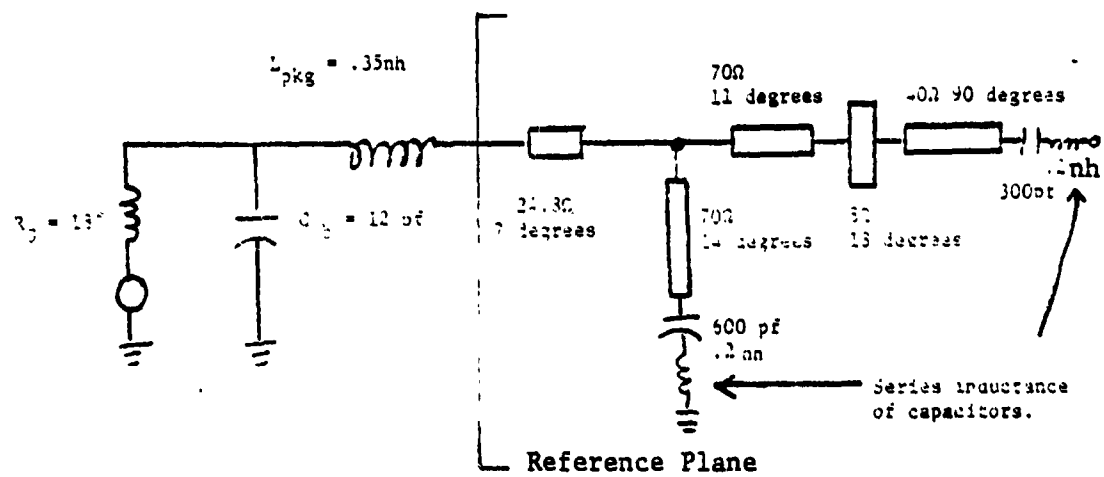
The previously generated transistor model was used for design of the first 18 watt, eight cell output matching network. When the quadrature couplers were finally selected for the final design, a quarter wave length transmission line transformer was integrated into the design to produce the 50 ohm match. Only the 50 ohm match will be discussed.

The first element of the output matching network was a series transmission line. This is necessary to provide a pad for soldering the transistor collector lead to the substrate. A shunt inductor was then used for matching and for feeding the collector voltage to the transistor. A low pass series transmission line and shunt capacitive stub were chosen to complete the remaining matching to approximately 25 ohms. Then a quarter wave length transformer was used to complete the 50 ohm match. A computer analysis program (MICAP) was then used to analyze the VSWR across the frequency range as the individual elements were varied. After much iteration the results shown in Table XVII were obtained.

This data shows that an acceptable match has been generated because output VSWRs of less than 1.2 to 1 have a negligible effect on transistor performance. A schematic of the optimized network is shown in Figure 44.

TABLE XVII. OUTPUT MATCHING NETWORK VSWR AND IMPEDANCE.
REFERENCE PLANE IS TRANSISTOR OUTPUT LEAD.

FREQUENCY	VSWR	Zin (REAL)	Zin (IMAGINARY)
550	1.31	18.3	4.9
600	1.16	17.3	2.5
650	1.13	16.4	1.4
700	1.15	15.8	0.9
750	1.15	15.7	0.6
800	1.14	15.8	0.3
850	1.11	16.2	0.05
900	1.08	16.6	-0.2
950	1.05	17.3	-0.5
1000	1.05	18.3	-0.8
1050	1.13	20.0	-1.2



All transmission lines are referenced to 800 MHz.

Figure 44. Output Matching Network.

2.4.5 Input Matching Network Design

The first input matching network was designed from the scaled single cell input model. As was the case for the output matching network the design was first made for a 25 ohm source impedance and then changed to 50 ohms when the quadrature coupler was substituted. Only the 50 ohm design is described.

The design was initiated by calculating a Fano matching network between the band center real impedance (0.65 ohms) and 50 ohms. The Fano network requires real impedances at both ends, a condition not satisfied by the complex chip impedance. The Fano network does, however, provide a useful starting point for computer optimization. The next step is modificatin of the network to absorb the complex parts of the chip impedance over the full design bandwidth. From the data gathered during characterization it appeared that a perfectically matched transistor would provide relatively flat gain; therefore,gain sloping with the input matching network was not attempted. Again the MICAP program was used for manual optimization. When the iteration was complete the predicted results shown in Table XVIII were obtained.

A schematic diagram of the completed input matching network is shown in Figure 45.

TABLE XVIII. CALCULATED INPUT IMPEDANCE FOR THE INPUT MATCHING NETWORK.

FREQUENCY MHz	VSWR (50Ω)	Z_{IN} REAL OHMS	Z_{IN} IMAGINARY OHMS
600	1.48	57.6	19.7
700	1.67	31.3	-8.5
800	1.69	29.6	-1.3
900	1.78	29.6	-9.9
1000	1.77	31.5	13.6

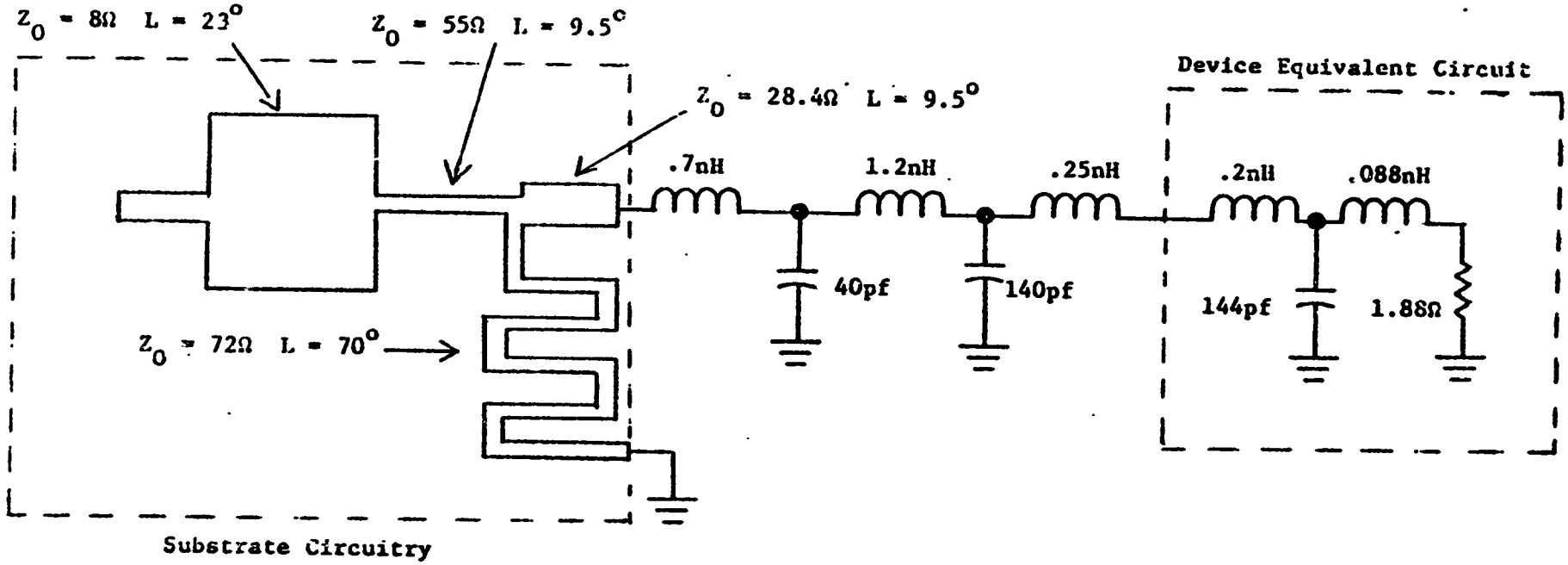


Figure 45. Input Matching Circuit.

Two of the input matching sections were placed within the microamp package. The last section is formed by the inductance of the emitter bond wires and a four section MOS capacitor placed at the appropriate location on the substrate. As the transistor chip was an eight cell device, the 0.25 nanohenry inductance actually consisted of eight bond wires connected in parallel. Because a four section MOS capacitor was used, two emitter bond wires were attached to each capacitor section. The four sections of the capacitor were then stitch bonded together to connect all eight cells in parallel at that point. The second matching section is formed by mounting two four section MOS capacitors at the appropriate distance from the previously discussed MOS capacitor. The capacitors were connected together with bond wires which are laid over a glass rod, placed midway between the two capacitors, to provide better dimensional control and rigidity. Figure 46 is a photograph of the microamp showing the internal construction. The two MOS capacitors were required for the second matching section because the second section bond wires were too short when laid out in line with the first bond wires. Angularity was required to correct this situation. Double bond wires were used for the second section to provide adequate current carrying capacity.

2.5 FIRST ENGINEERING SAMPLES.

2.5.1 First Engineering Sample Description

The first engineering samples were single transistor amplifiers. These samples were fabricated to test the matching network design accuracy and determine the changes required for optimization. As the quadrature combiners were not required for these samples and metal adhesion problems were being encountered, the substrates were fabricated on common rough surfaced alumina.

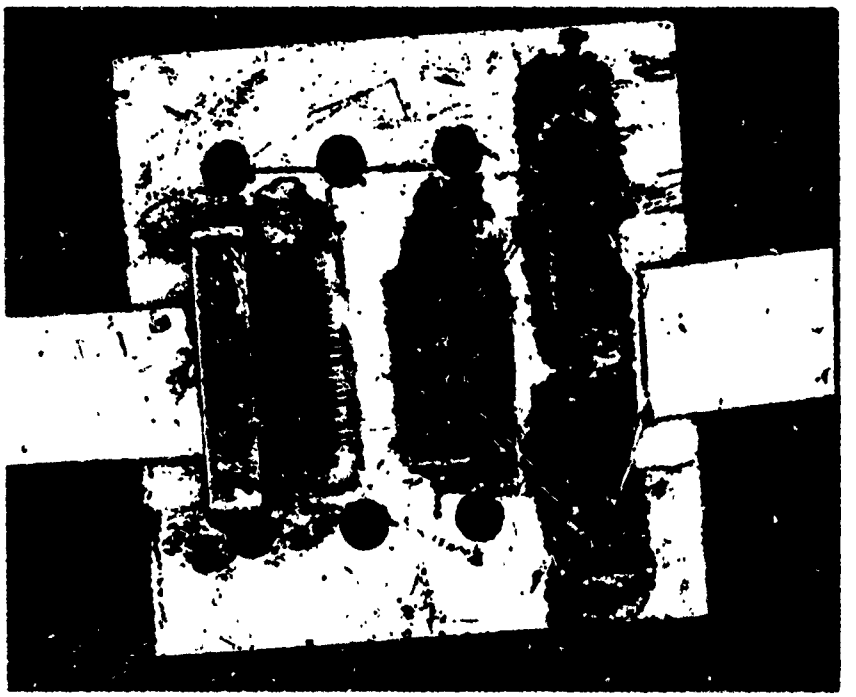


Figure 46. MICroAMP Internal Construction.

2.5.2 Test Results First Engineering Samples.

The output matching network of the first amplifier was pre-tuned using a network analyzer so that the best possible match of measured impedance data to calculated impedance data (Section 2.4.2, Table XII) was obtained. These results are shown in Figure 47. The microamp^{R} transistor was installed. Upon the application of power to the amplifier full output power was obtained across the entire 600 MHz to 1000 MHz frequency range, however, the collector efficiency was low at some frequencies. Further testing showed that the direct current voltage drop in both of the printed thin film gold collector feed chokes and the emitter return choke was excessive. The microamp was operating from 25.5 volts when 28 volts was applied to the amplifier. To cure the problem a five-mil gold wire was parallel gap welded along the entire length of all three chokes, and the substrates for the second set of engineering samples were returned for additional gold plating. Minor readjustment to the input and output networks produced the results shown in Table XIX.

The second and third amplifiers were adjusted optically under a microscope to the same line lengths and capacitive areas that produced the final results for the first amplifier. Minor readjustment of the networks produced the results shown in Table XIX. Note that amplifier number three utilizes a microamp transistor from a different lot and wafer than the first two amplifiers.

2.6 SECOND ENGINEERING SAMPLES

2.6.1 Second Engineering Sample Description

The second engineering samples were fabricated to confirm the elimination of the problems uncovered during the fabrication and test of the first engineering samples. These samples were used to evaluate the transistor and the required external matching circuitry.

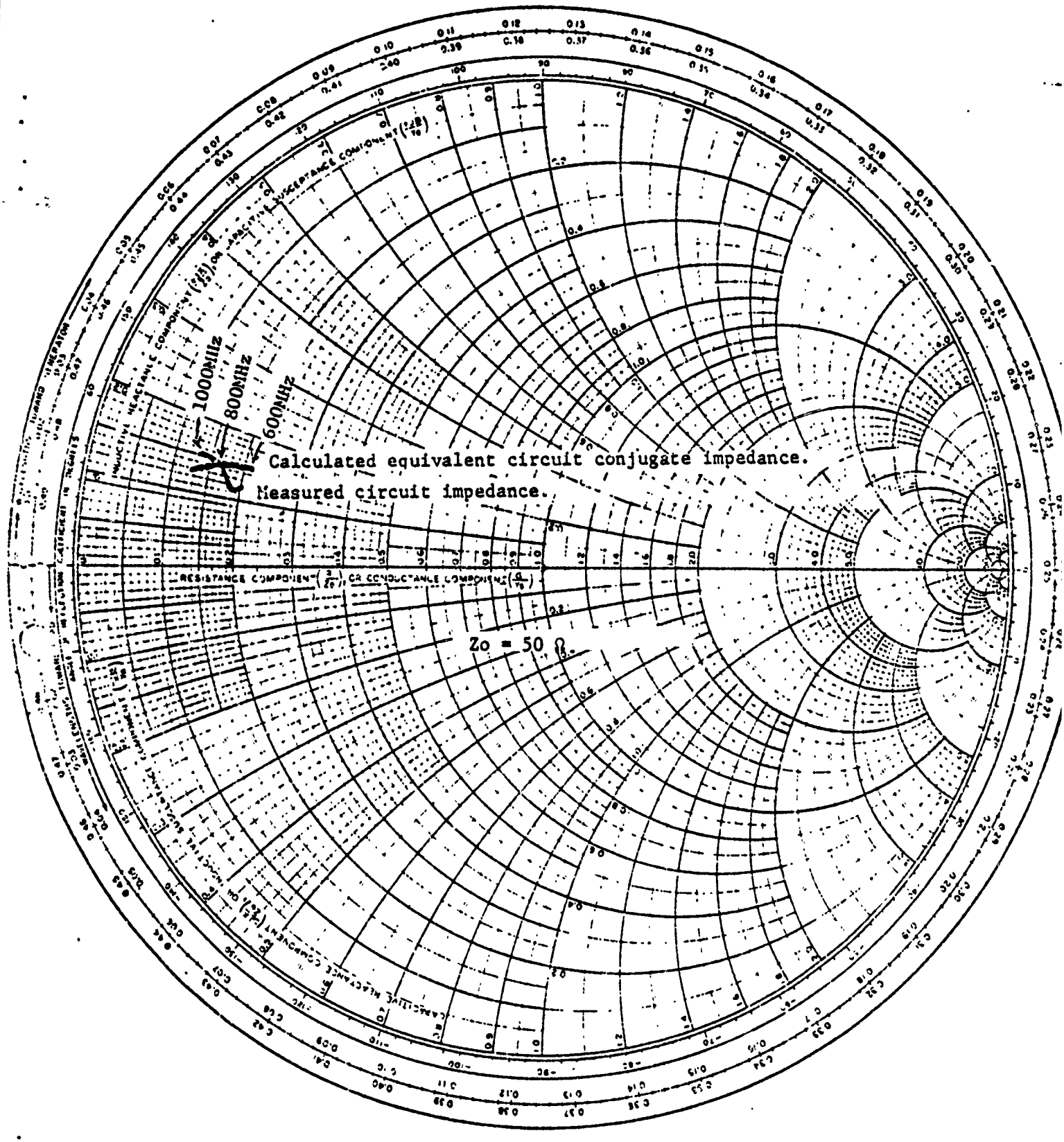


Figure 47. Comparison of Measured Output Circuit Impedance to Calculated Equivalent Circuit Conjugate Impedance.

TABLE XIX. PERFORMANCE DATA FOR THE FIRST SET OF ENGINEERING SAMPLES.

	f(MHz)	P_{IN}(Watts)	P_O(Watts)	I_C(Amps)	(REF) P(Watts)
UNIT 1	600	3.05	18	1.10	.8
	700	2.35	18	1.14	.27
	800	2.20	18	1.18	-
	900	2.40	18	1.16	-
	1000	2.75	18	1.11	.1
UNIT 2	600	2.65	18	1.10	.56
	700	2.30	18	1.18	.22
	800	2.20	18	1.23	-
	900	2.30	18	1.18	-
	1000	2.80	18	1.14	.22
UNIT 3	600	2.70	18	1.10	.80
	700	2.25	18	1.10	.34
	800	2.00	18	1.22	-
	900	2.20	18	1.20	.C5
	1000	2.55	18	1.22	.12

Vcc = 28V

Units 1 and 2 were MW1-10 #24 wafer.
Unit 3 was MW1-10 #33 wafer.

The substrates were the same as those used for the first engineering samples and were processed at the same time. Additional plating was built up on the second set of engineering sample substrates to

alleviate the voltage drop problems uncovered during test of the first engineering samples. A total of twelve microns of gold thickness was applied to the second engineering sample substrates; six microns of gold was applied to the first engineering samples. This buildup was possible becaure the second engineering samples did not contain the quadrature couplers which limit plating thickness.

2.6.2 Test Results Second Engineering Samples.

All three amplifiers were pre-tuned to the calculated impedance values by using a network analyzer. The procedure used was identical to that used for the first engineering sample amplifiers. After inserting the microamp^{R} transistors, it was determined that although the voltage drops were less than the previous amplifiers, they were still too large for achievement of the desired performance. A one volt drop still existed in the three chokes. (VCC secondary choke, VCC primary choke, and emitter feed choke.) To correct the problem, the parallel gap welder was again used to weld a five mil gold wire along the entire length of all three chokes.

The performance shown in Table XX was attained. The three amplifiers were shipped with no further adjustment. The difference in performance shown in this table is a result of the variations in both the microamp transistor characteristics and the batch processed substrate characteristics.

As an extra set of substrates was available, a seventh amplifier was constructed. Considerable time was spent in trying to improve the efficiency in the middle of the band without sacrificing too much efficiency at the band edges. The final performance of

TABLE XX. PERFORMANCE DATA FOR THE SECOND SET OF ENGINEERING SAMPLES.

	f(MHz)	P_{IN}(Watts)	P_O(Watts)	I_C(Amps)	(REF) P(Watts)
UNIT 4	600	2.50	18	1.07	.54
	700	2.20	18	1.16	.28
	800	2.15	18	1.24	.04
	900	2.15	18	1.15	-
	1000	2.40	18	1.17	-
UNIT 5	600	2.60	18	1.04	.42
	700	2.25	18	1.10	.26
	800	2.25	18	1.23	.04
	900	2.35	18	1.21	.02
	1000	2.20	18	1.08	-
UNIT 6	600	2.40	18	1.07	.47
	700	2.20	18	1.11	.35
	800	2.05	18	1.25	.03
	900	2.20	18	1.24	-
	1000	2.20	18	1.16	-

Vcc = 28V

this amplifier is shown in Table XXI. Note that the goal was achieved. This performance was obtained by increasing the length of the series collector choke by about three mils. At this time it was not known whether this improvement can be effected on a batch basis, or whether individual tuning will be required.

TABLE XXI. PERFORMANCE OF THE SEVENTH AMPLIFIER.

f(MHz)	P_{IN}(Watts)	P_{IN}(REF)	P_O(Watts)	I_C(Amps)
600	2.60	0.54	18	1.08
650	2.30	0.38	18	1.10
700	2.10	0.15	18	1.16
750	2.00	0.04	18	1.16
800	2.05	-	18	1.16
850	2.10	-	18	1.15
900	2.10	-	18	1.12
950	2.20	-	18	1.14
1000	2.30	0.03	18	1.08

Vcc = 28V

2.7 EVALUATION OF THE MW2000 TRANSISTOR CELL FOR USE IN THE CONTRACT AMPLIFIER.

2.7.1 Justification for Use of the MW2000 Parameter.

Although the MW1 parameter was successfully used to produce the first and second engineering sample amplifiers, problems were experienced with the availability of dice having the required output power capability to consistently produce amplifiers. The MW2000 cell had been developed to alleviate this problem for the standard micro-amp line of transistors and was slated to become the standard microwave die. Since the MW1 device was being phased out, it was decided to evaluate the new cell for the contract amplifier.

2.7.2 Preliminary MW2000 Test Results.

Transistors were built to the MW1 part drawings and tested on a spot frequency basis using stub tuners. This device was not ballasted and was obtained from an early prototype lot of devices. It exhibited power gain in excess of 10 dB and acceptable efficiency from 700 MHz to 1000 MHz. A mismatch in the collector circuit prevented meaningful testing at the low frequency end of the band. Because the device was not fully representative of the final part intended for use in this frequency range, only a small effort in retuning the amplifier was expended and only limited results were obtained. These, however, indicated that minor modifications to the output matching network would allow the use of the new transistor, and result in performance superior to that of the old transistor.

2.7.3 MW2000 Test Results.

The MW2000 transistor contained eight cells, which were capable of producing 25 per cent more power than the older MW1 device. At the same time, the C_{ob} of the new device is approximately the same as for the old device. Little retuning of the matching circuitry was required to produce the results shown in Table XXII. The same device, when tested on a spot frequency basis, exhibited efficiencies in the 58 to 60 per cent region, indicating that the broadband performance is very good. Increasing the second input matching section inductance improved the input VSWR considerably.

TABLE XXII. PERFORMANCE OF AN EIGHT CELL MW2000 DEVICE IN THE CONTRACT CIRCUIT.

f(MHz)	P_{IN} WATTS	P_{REF} WATTS	I_C AMPS	Gain dB	Eff. %
600	3.1	1.5	1.27	8.1	56
700	2.1	0.6	1.18	9.8	60
800	2.1	0.25	1.28	9.8	56
900	2.2	0.25	1.22	9.6	58
1000	2.2	0.55	1.22	9.6	58

V_{CC} = 28V P_{OUT} = 20 Watts

Three engineering sample amplifiers were constructed from transistors containing the increased inductance. The performance of the three amplifiers is illustrated by Tables XXIII and XXIV. It should be noted that good performance was obtained from transistors from two different processing lots.

The single ended amplifiers meet the contract requirements of power output and efficiency, however, the gain of the amplifiers is slightly lower than specified. Because the narrow band gain of the transistor is approximately 11dB, achievement of the specified gain would require an increase in the number of impedance matching sections in both the input and output networks. Such an increase is not desiragle due to the increased complexity and size of the amplifier. This loss in gain from the narrow band case is a reasonable compromise for the bandwidth required for the contract effort.

TABLE XXIII. PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIERS #1 AND #2.

f(MHz)	P_{IN} WATTS	I_C AMPS	P_{REF} WATTS	EFF. %	
600	2.70	1.19	0.49	60	Amplifier #1
650	2.27	1.15	0.15	62	
700	2.26	1.15	0.08	62	
750	2.44	1.22	0.15	58	
800	2.60	1.29	0.27	55	
850	2.70	1.29	0.31	55	
900	2.65	1.24	0.26	58	
950	2.55	1.18	0.18	60	
1000	2.96	1.22	0.17	58	
600	2.83	1.20	0.58	59	Amplifier #2
650	2.40	1.16	0.31	62	
700	2.38	1.18	0.14	60	
750	2.39	1.24	0.17	58	
800	2.55	1.26	0.25	57	
850	2.56	1.28	0.27	56	
900	2.65	1.28	0.24	56	
950	2.70	1.30	0.50	55	
1000	2.55	1.22	0.05	58	

P_{OUT} = 20 WATTS

V_{CC} = 28 VOLTS

Source = MW 2000-11#B

TABLE XXIV. PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER #3.

f(MHz)	P_{IN} WATTS	I_C AMPS	P_{REF} WATTS	EFF. %
600	2.21	1.24	0.47	58
650	1.90	1.23	0.28	58
700	1.84	1.29	0.12	55
750	1.89	1.30	0.11	55
800	2.00	1.33	0.13	54
850	2.05	1.32	0.17	54
900	2.05	1.32	0.14	54
950	2.20	1.33	0.10	54
1000	2.20	1.30	0.03	55

P_{OUT} = 20 WATTS
V_{CC} = 28 VOLTS
Source = MW 2000-9#C

2.7.4 QUADRATURE COMBINED AMPLIFIER PERFORMANCE.

Two amplifiers were built and tested. The test results of the amplifiers are shown in Table XXV. A pair of quadratures (Standard #2 and #3) used for previous coupler testing were used to combine the two amplifiers. The performance obtained from the combined amplifier is shown in Table XXVI. The results of this test correlate with the independent testing done previously on the quadrature couplers.

The relatively poor performance at the high end of the band is caused by excessive coupler length. Improved performance is expected when the matching circuits and shortened couplers are all fabricated on the same substrate, since the number of connector to microstrip interfaces will be drastically reduced. Thus, the VSWR presented to the transistors should be improved.

The quadrature combined amplifier demonstrated that individual amplifiers were capable of being combined to produce a useful assembly.

2.8 THIRD ENGINEERING SAMPLES

2.8.1 Third Engineering Sample Description

The third engineering sample amplifiers were quadrature combined amplifiers intended to evaluate the entire substrate containing the matching circuitry, micro-amp transistors, quadrature combiners, difference port resistors. The substrates were mounted on brass blocks which allowed the attachment of the input and output connectors. The third engineering sample amplifiers used MW2000 transistors and demonstrated the electrical performance that could be expected from the final item.

TABLE XXV. INDEPENDENT PERFORMANCE OF AMPLIFIERS 1 AND 2 IN THE QUADRATURE COMBINED PAIR.

f(MHz)	P_{IN} WATTS	I_C ADC	P_{REF} WATTS	EFF. %	
600	2.38	1.16	0.44	55	AMPLIFIER #1
650	1.90	1.06	0.25	60	
700	1.72	1.02	0.18	64	
750	1.65	1.07	0.07	60	
800	1.74	1.12	0.11	57	
850	1.85	1.16	0.17	55	
900	1.98	1.17	0.12	55	
950	1.95	1.17	0.07	55	
1000	1.90	1.10	0.06	58	
600	2.34	1.15	.45	56	AMPLIFIER #2
650	1.79	1.03	.17	62	
700	1.61	.98	.10	65	
750	1.71	1.02	.08	63	
800	1.79	1.08	.17	59	
850	1.96	1.14	.20	56	
900	2.08	1.17	.10	55	
950	2.06	1.17	.02	55	
1000	1.97	1.06	.05	60	

P_{OUT} = 18 WATTS
V_{CC} = 28 VOLTS

TABLE XXVI . PERFORMANCE OF THE QUADRATURE COMBINED AMPLIFIER.

f(MHz)	P_{IN} WATTS	$P_{DIF\ IN}$ WATTS	P_{REF} WATTS	I_{C1} ADC	I_{C2} ADC	$P_{DIF\ OUT}$ WATTS
600	4.4	0.90	0.0	1.05	1.05	1.90
650	3.5	0.36	0.0	1.02	0.94	1.10
700	3.5	0.23	0.04	1.08	0.92	1.60
750	3.4	0.05	0.08	1.15	0.95	1.40
800	3.5	0.08	0.10	1.14	1.00	0.50
850	3.4	0.18	0.05	1.02	1.00	0.0
900	3.5	0.25	0.06	1.00	1.05	1.20
950	4.6	0.10	0.06	1.17	1.21	5.30
1000*	5.0	0.09	0.20	1.13	1.20	4.80

P_{OUT} = 30 WATTS
V_{CC} = 28 VOLTS
*P_{OUT} = 27 WATTS

2.8.2 Test Results, Third Engineering Sample Amplifiers

The third engineering sample test results (Tables XXVII through XXX show that the amplifier performance meets the contract requirements for output power and efficiency, however, the gain is less than the contract requirements of 10 dB. Optimization of the input match will result in increased gain, however, it is doubtful that the contract figure can be met by the amplifier. The difference between Ic1 and Ic2 is an indication of the change in quadrature coupling across the frequency range. The larger difference noted in engineering sample number 2 was correlated with excessive line widths and narrower spacing between lines in the couplers used in that amplifier. The control of these variations is discussed in Sections 2.2.5 and 2.3.2.

TABLE XXVII . TEST DATA FROM ENGINEERING SAMPLE NUMBER 1.

f (MHz)	P_{IN} WATTS	P_{OUT} WATTS	I_{C1} ADC	I_{C2} ADC	η %
600	3.83	30	1.12	.94	52.0
650	3.43	30	1.09	.96	52.3
700	3.19	30	1.04	.94	54.1
750	2.84	30	1.06	1.03	51.3
800	2.89	30	1.02	1.09	50.8
850	2.91	30	.96	1.10	52.0
900	3.11	30	.96	1.06	53.0
950	3.19	30	1.02	.97	53.8
1000	3.43	30	1.07	.89	54.7

Note: V_{CC} = 28 Volts

TABLE XXVIII. TEST DATA FROM ENGINEERING SAMPLE NUMBER 2.

f (MHz)	P_{IN} WATTS	P_{OUT} WATTS	I_{C1} ADC	I_{C2} ADC	η %
600	5.20	30	1.00	1.04	52.5
650	4.21	30	1.02	.96	54.1
700	3.79	30	1.02	.86	57.0
750	3.55	30	1.10	.84	55.2
800	3.30	30	1.15	.91	52.0
850	3.42	30	1.15	.95	51.0
900	3.50	30	1.12	.95	51.7
950	3.61	30	1.06	.98	52.5
1000	3.79	30	.98	1.02	53.6

Note: V_{CC} 28 Volts

TABLE XXIX. TEST DATA FROM ENGINEERING SAMPLE NUMBER 3.

f (MHz)	P_{IN} WATTS	P_{OUT} WATTS	I_{C1} ADC	I_{C2} ADC	η %	G_p dB
600	4.33	30	.97	.95	55.8	8.4
650	3.75	30	.92	.98	56.3	9.0
700	3.55	30	.92	.98	56.4	9.3
750	3.17	30	1.02	1.00	53.0	9.8
800	3.09	30	1.01	1.06	51.8	9.9
850	3.11	30	.98	1.12	51.0	9.8
900	3.21	30	.94	1.10	52.5	9.7
950	3.19	30	.96	1.06	53.0	9.7
1000	3.43	30	1.02	1.01	52.8	8.7

Note: V_{CC} = 28 Volts

TABLE XXX . TEST DATA FROM ENGINEERING SAMPLE NUMBER 4.

f (MHz)	P_{IN} WATTS	P_{OUT} WATTS	I_{C1} ADC	I_{C2} ADC	η %	G_p dB
600	5.45	30	1.04	1.01	52.3	7.4
650	4.58	30	1.10	.91	53.3	8.2
700	4.29	30	1.09	.91	53.6	8.4
750	3.82	30	1.07	1.00	51.8	8.9
800	3.50	30	1.13	.98	50.8	9.3
850	3.30	30	1.14	.93	51.8	9.6
900	3.30	30	1.11	.88	53.8	9.6
950	3.29	30	1.10	.90	53.4	9.6
1000	3.67	30	1.06	.98	52.5	9.1

Note: V_{CC} = 28 Volts

2.8.3 Test Results, Amplifiers Built in Brass Housing Models.

Two additional amplifiers were built in the brass model housings. These amplifiers fully represent the finished product except for the hermetic connectors. In an effort to achieve more gain flatness across the band a modified internal input matching network configuration was used. Examination of the test data (Tables XXXI and XXXII) shows that while the gain has been improved at the low end of the band, the gain is excessively low at the high frequency end of the band which is the opposite condition from that exhibited by the third engineering sample amplifiers. Therefore, the optimum match is between the two tried thus far.

Amplifier Number 5 was tested for a 3 to 1 VSWR through a complete 360° at both 600 MHz and 1000 MHz. This test was made at 30 watts output at 28 volts dc supply voltage. The amplifier withstood the VSWR at 1000 MHz, but one transistor failed during the 600 MHz test. The failed transistor was replaced and the replacement failed. This failure has been attributed to an abnormal secondary breakdown mechanism associated with the lot of transistors used for these amplifiers. New transistor lots were started to correct the problem. The transistors in both amplifiers were replaced with units from the fourth engineering sample amplifier, and the performance optimized at 80° C. baseplate temperature. The amplifiers' performances are shown in Tables XXXIII through XXXVI . It should be noted that the contract requirements have been met at the elevated temperature with the exception of module gain.

TABLE XXXI . TEST DATA FROM ENGINEERING SAMPLE NUMBER 5.

f (MHz)	P_{IN} WATTS	P_{OUT} WATTS	I_C (ADC)	V_{CC} (VDC)	P_{REF} (MW)	η %	G_P dB
600	3.6	30	1.90	28	30	56.4	9.2
650	3.3	30	1.85	28	35	57.9	9.6
700	3.1	30	1.86	28	30	57.6	9.9
750	3.0	30	2.04	28	25	52.5	10.0
800	3.2	30	2.11	28	28	50.8	9.7
850	3.6	30	2.12	28	32	50.5	9.5
900	3.6	30	2.07	28	15	51.8	9.2
950	3.9	30	2.01	28	-	53.3	8.9
1000	4.4	30	2.07	28	25	51.8	8.3

TABLE XXXII . TEST DATA FROM ENGINEERING SAMPLE NUMBER 6.

f (MHz)	P_{IN} WATTS	P_{OUT} WATTS	I_C (ADC)	V_{CC} (VDC)	P_{REF} (MW)	η %	G_P dB
600	3.7	30	1.88	28	30	57.0	9.1
650	3.6	30	1.91	28	30	56.1	9.2
700	3.3	30	1.92	28	18	55.8	9.6
750	3.2	30	2.08	28	13	51.5	9.7
800	3.2	30	2.13	28	17	50.3	9.7
850	3.4	30	2.13	28	27	50.3	9.5
900	3.5	30	2.06	28	3	52.0	9.3
950	3.7	30	2.04	28	-	52.5	9.1
1000	4.3	30	2.02	28	3	53.0	8.4

TABLE XXXIII. PERFORMANCE OF REWORKED AMPLIFIER NO. 5 AT 25° C.

f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	η %	G_P (dB)
600	4.60	42	1.92	55.3	8.14
650	3.90	10	1.87	57.2	8.86
700	3.55	26	1.88	57.0	8.45
750	3.15	36	1.95	54.9	9.52
800	3.05	12	1.98	54.1	9.92
850	3.20	0	2.00	53.6	9.72
900	3.40	1	1.99	53.8	9.46
950	3.30	9	1.86	57.6	9.59
1000	4.60	36	1.75	61.2	8.14

V_{CC} = 28 Volts P_O = 30 Watts T_A = 25° Centigrade

TABLE XXXIV. PERFORMANCE OF REWORKED AMPLIFIER NO. 5 AT 80° C.

f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	η %	G_P (dB)
600	4.48	44	2.02	53.0	8.26
650	3.78	22	1.96	54.7	9.00
700	3.42	39	1.98	54.1	9.43
750	3.05	46	2.04	53.0	9.93
800	3.00	20	2.07	51.8	10.00
850	3.20	9	2.10	51.0	9.72
900	3.38	10	2.12	50.5	9.48
950	3.37	10	2.00	53.6	9.49
1000	3.83	50	2.04	53.0	8.94

V_{CC} = 28 Volts P_O = 30 Watts T_A = 80° Centigrade

TABLE XXXV . PERFORMANCE OF REWORKED AMPLIFIER NO. 6 AT 25° C.

f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	η %	G_P (dB)
600	4.54	42	1.92	55.8	8.2
650	4.20	10	1.87	57.3	8.5
700	3.78	26	1.88	57.0	9.00
750	3.42	36	1.95	54.9	9.43
800	3.55	12	1.98	54.1	9.27
850	3.52	0	2.00	53.6	9.31
900	3.57	1	1.99	53.8	9.24
950	3.62	9	1.86	57.6	9.18
1000	4.01	36	1.75	61.2	8.74

V_{CC} = 28 Volts P_O = 30 Watts T_A = 25° Centigrade

TABLE XXXVI . PERFORMANCE OF REWORKED AMPLIFIER NO. 6 AT 80° C.

f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	η %	G_P (dB)
600	4.23	54	1.92	55.8	8.51
650	3.90	36	1.96	54.7	8.86
700	3.54	30	1.93	55.5	9.28
750	3.31	51	2.03	52 8	9.57
800	3.20	48	2.08	51.3	9.72
850	3.20	42	2.10	51.0	9.72
900	3.38	0	2.07	51.8	9.48
950	3.57	0	2.03	52.8	9.24
1000	4.25	39	2.12	50.5	8.49

V_{CC} = 28 Volts P_O = 30 Watts T_A = 25° Centigrade

2.9 FOURTH ENGINEERING SAMPLE AMPLIFIERS.

2.9.1 Fourth Engineering Sample Description.

The fourth engineering sample amplifiers were quadrature combined amplifiers built in nickel plated aluminum housings designed for solder hermetic sealing.

These amplifiers represent the finished product in all respects except for the hermeticity requirement. Hermeticity could have been achieved had the hermetic connectors been received at a reasonable date. The transistors used for these amplifiers were fabricated with the internal input matching network configuration at the value indicated as optimum by the results of the third engineering sample amplifiers and the brass housing amplifiers.

2.9.2 Test Results Fourth Engineering Sample Amplifiers.

These modules were tested for gain, output power, efficiency, input return loss, and relative phase. All of the parameters, except relative phase, were tested both at room temperature and at 80°C. The test results are shown in Tables XXXVII through XLV . The marginal efficiency at elevated temperatures is caused by poor thermal contact between the transistor flange and the housing. This has been verified by measuring the transistor flange temperature, which was 20°C. higher than the heatsink temperature. This temperature difference is produced because the surface finish on the housing floor is too rough to provide good thermal contact to the transistor flange. This situation has been corrected by adding a surface finish specification to the housing drawing. In addition, a thermal conductive compound will be used to interface the transistor flanges to the mounting surface.

The gain and phase variation data between the five modules has been tabulated and is shown in Table XLVI . The modules meet the phase variation requirements of the contract, but the gain

was low at the band edges. However, the response curve of the amplifier has been centered with the gain rolling off at both the high and low ends of the frequency range. Testing the fifteen pre-production amplifiers will give better insight as to the achievable amplifier gain.

TABLE XXXVII . PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 7 AT ROOM TEMPERATURE.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	REL PHASE	G_P (dB)
600	4.52	2.13	50.3	7	-68°	8.22
650	3.74	2.00	53.6	6	$+108^{\circ}$	9.04
700	3.58	2.00	53.6	13	-73°	9.23
750	3.36	2.10	51.0	6	$+117^{\circ}$	9.51
800	3.32	2.14	50.1	2	-60°	9.56
850	3.37	2.12	50.5	15	$+126^{\circ}$	9.49
900	3.46	2.12	50.5	18	-57°	9.38
950	3.43	2.07	51.8	6	$+125^{\circ}$	9.42
1000	3.80	2.02	53.0	16	-72°	8.97

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XXXVIII. PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 7 AT 80°C.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	G_P (dB)
600	4.58	2.11	50.8	6	8.16
650	3.74	1.98	54.1	6	9.04
700	3.58	1.94	55.2	13	9.23
750	3.46	2.10	51.0	6	9.38
800	3.42	2.12	50.5	2	9.43
850	3.64	2.15	49.8	14	9.16
900	3.64	2.13	50.3	18	9.16
950	3.72	2.06	52.0	8	9.07
1000	3.79	1.92	55.8	12	8.97

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE.XXXIX. PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 8 AT ROOM TEMPERATURE.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	REL PHASE	G_P (dB)
600	4.64	2.03	52.8	24	-68°	8.11
650	3.86	1.96	54.7	20	+112°	8.90
700	3.25	1.90	56.4	30	-70°	9.65
750	3.15	1.96	54.7	38	+115°	9.79
800	3.14	2.07	51.8	23	-60°	9.80
850	3.37	2.10	51.0	8	+127°	9.49
900	3.28	2.12	50.5	2	-53°	9.61
950	3.43	2.08	51.5	0	+129°	9.42
1000	3.68	1.98	54.1	18	-59°	9.11

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XL . PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 8 AT 80°C.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	G_P (dB)
600	4.52	2.07	51.8	22	8.22
650	3.74	2.01	53.3	17	9.04
700	3.14	1.96	54.7	28	9.80
750	3.10	2.02	53.0	40	9.86
800	3.14	2.10	51.0	24	9.80
850	3.32	2.13	50.3	9	9.56
900	3.35	2.17	49.4	6	9.52
950	3.51	2.14	50.1	17	9.32
1000	3.91	2.08	51.5	38	8.85

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XLI . PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 9 AT ROOM TEMPERATURE.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	REL PHASE	G_P (dB)
600	3.94	2.13	50.3	15	-73°	8.81
650	3.28	1.98	54.1	12	$+107^{\circ}$	9.61
700	3.14	1.97	54.4	16	-77°	9.80
750	3.15	2.07	51.8	37	$+112^{\circ}$	9.79
800	3.14	2.10	51.0	70	-63°	9,80
850	3.37	2.10	51.0	105	$+123^{\circ}$	9.49
900	3.55	2.14	50.1	120	-58°	9.27
950	3.72	2.04	52.5	70	$+125^{\circ}$	9.07
1000	3.68	1.96	54.7	10	-70°	9.11

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XLII . PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 9 AT 80°C.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	G_P (dB)
600	3.83	2.14	50.1	20	8.94
650	3.28	2.01	53.3	16	9.61
700	3.02	2.00	53.6	22	9.97
750	3.04	2.08	51.5	42	9.94
800	3.13	2.11	50.8	74	9.82
850	3.37	2.12	50.5	110	9.50
900	3.64	2.19	48.9	125	9.16
950	3.63	2.08	51.5	72	9.17
1000	4.26	2.08	51.5	10	8.48

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XLIII. PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 10 AT ROOM TEMPERATURE.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	REL PHASE	G_P (dB)
600	4.29	2.02	53.0	24	-64°	8.45
650	3.51	1.90	56.4	14	+114°	9.32
700	3.25	1.87	57.3	18	-69°	9.65
750	3.15	1.94	55.2	10	+118°	9.79
800	3.04	2.08	51.5	2	-59°	9.94
850	3.19	2.10	51.0	21	+128°	9.73
900	3.37	2.10	51.0	28	-51°	9.49
950	3.43	1.98	54.1	11	+131°	9.42
1000	3.91	1.90	56.4	2	-58°	8.85

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XLIV. PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 10 AT 80°C.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	G_P (dB)
600	3.94	2.06	52.0	20	8.82
650	3.28	1.95	54.9	13	9.61
700	3.02	1.91	56.1	20	9.97
750	2.94	2.01	53.3	11	10.1
800	2.85	2.10	51.0	1	10.2
850	3.00	2.12	50.5	20	10.0
900	3.28	2.13	50.3	24	9.61
950	3.33	2.03	52.8	7	9.55
1000	4.02	2.07	51.8	4	8.73

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XLV . PERFORMANCE OF ENGINEERING SAMPLE AMPLIFIER NUMBER 11 AT ROOM TEMPERATURE.

f (MHz)	P_{IN} WATTS	I_C (ADC)	η %	P_{REF} (MW)	REL PHASE	G_P (dB)
600	4.13	2.04	52.5	6	-67°	8.51
650	3.51	1.93	55.5	7	$+112^\circ$	9.32
700	3.42	1.96	54.7	14	-69°	9.43
750	3.26	2.09	51.3	10	$+122^\circ$	9.64
800	2.99	2.12	50.5	6	-54°	10.00
850	3.14	2.12	50.5	17	$+132^\circ$	9.80
900	3.28	2.10	51.0	23	-48°	9.61
950	3.28	2.06	52.0	11	$+132^\circ$	9.61
1000	3.45	1.98	54.1	23	-59°	9.39

P_O = 30 Watts

V_{CC} = 28 Volts

TABLE XLVI . MEASURED GAIN AND PHASE VARIATIONS FOR THE FIVE ENGINEERING SAMPLE AMPLIFIERS.

f (MHz)	P_I MIN	P_I MAX	MAX / MIN	Δ DB	θ MAX DEGREES	θ MIN DEGREES	$\Delta\theta$ DEGREES
600	3.94	4.64	1.18	.71	-64	-68	4
650	3.28	3.86	1.18	.71	114	107	7
700	3.14	3.58	1.14	.57	-69	-77	8
750	3.13	3.36	1.07	.28	122	112	10
800	2.99	3.32	1.11	.45	-54	-63	9
850	3.14	3.37	1.07	.31	132	123	9
900	3.28	3.55	1.08	.34	-48	-58	10
950	3.28	3.72	1.13	.55	132	125	7
1000	3.45	3.91	1.13	.54	-58	-72	14

2.9.3 Combining and Efficiency Loss Calculations.

The transistors used for fabrication of the fourth engineering sample amplifiers were tested individually and matched before final assembly. The data gathered on the parts is shown in Tables XLVII through LI .

If no losses were encountered in combining the pairs of transistors, the expected efficiency from the amplifier is:

$$\eta_1 = \frac{P_1}{P_{DC1}} \qquad (1)$$

where: η_1 = the expected efficiency neglecting losses,

P_1 = the sum of the two output powers from the individual transistors,

P_{DC1} = the sum of the two dc input powers from the two transistors.

The efficiency of the combined amplifier may be similarily described as:

$$\eta_2 = \frac{P_0}{P_{DC2}} \qquad (2)$$

where: η_2 = the measured efficiency of the combined amplifier,

P_0 = the combined amplifier output power,

P_{DC2} = the dc input power to the combined amplifier.

Assuming that the efficiency is constant over the power range necessary to complete the calculations,

$$\frac{P_1}{P_{DC1}} = \frac{P_A}{P_{DC2}}$$

where: P_A = the total power produced by the transistors to produce P_0 at the output connector.

Rearranging terms,

$$\frac{P_A}{P_1} = \frac{P_{DC2}}{P_{DC1}}$$

TABLE XLVII . INDIVIDUAL PERFORMANCE OF THE TRANSISTORS INSTALLED IN AMPLIFIER NO. 7.

	TRANSISTOR #1			TRANSISTOR #2		
f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)
600	2.30	340	1.10	2.25	300	1.10
700	1.90	100	1.08	1.90	70	1.12
800	2.10	60	1.14	2.15	60	1.15
900	2.30	150	1.07	2.30	100	1.12
1000	1.80	20	1.05	1.90	20	1.15

V_{CC} = 28 Volts

P_O = 18 Watts

TABLE XLVIII. INDIVIDUAL PERFORMANCE OF THE TRANSISTORS INSTALLED IN AMPLIFIER NO. 8.

	TRANSISTOR #4			TRANSISTOR #7		
f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)
600	2.50	360	1.10	2.20	750	1.02
700	2.05	50	1.10	1.90	40	1.00
800	2.40	100	1.14	2.30	80	1.12
900	2.50	130	1.10	2.50	80	1.10
1000	2.10	40	1.08	2.15	120	1.05

V_{CC} = 28 Volts

P_O = 18 Watts

TABLE XLIX. INDIVIDUAL PERFORMANCE OF THE TRANSISTORS INSTALLED IN AMPLIFIER NO. 9.

	TRANSISTOR #11			TRANSISTOR #20		
f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)
600	1.93	550	1.05	2.05	280	1.02
700	1.75	30	1.04	1.75	100	1.02
800	2.05	60	1.14	2.00	60	1.12
900	2.15	50	1.12	1.95	110	1.10
1000	1.90	130	1.07	1.85	30	1.10

V_{CC} = 28 Volts

P_O = 18 Watts

TABLE L . INDIVIDUAL PERFORMANCE OF THE TRANSISTORS INSTALLED IN AMPLIFIER NO. 10.

	TRANSISTOR #9			TRANSISTOR #14		
f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)
600	2.15	700	1.07	2.20	900	1.05
700	1.85	50	1.02	1.85	80	1.04
800	2.15	50	1.16	2.10	70	1.14
900	2.20	60	1.14	2.25	120	1.13
1000	1.90	80	1.08	1.85	50	1.10

V_{CC} = 28 Volts

P_O = 18 Watts

TABLE LI INDIVIDUAL PERFORMANCE OF THE TRANSISTORS INSTALLED IN AMPLIFIER NO. 11.

	TRANSISTOR #5			TRANSISTOR #6		
f (MHz)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)	P_{IN} WATTS	P_{REF} (MW)	I_C (ADC)
600	2.30	380	1.10	2.30	320	1.13
700	1.85	110	1.10	1.90	90	1.12
800	2.00	50	1.10	2.15	70	1.15
900	2.15	20	1.06	2.30	120	1.11
1000	1.80	20	1.08	1.90	50	1.10

V_{CC} = 28 Volts

P_O = 18 Watts

from equations 1 and 2,

$$P_{DC1} = \frac{P_1}{\eta_1} \text{ and } P_{DC2} = \frac{P_0}{\eta_2}$$

so,

$$\frac{P_A}{P_1} = \frac{\frac{P_0}{\eta_2}}{\frac{P_1}{\eta_1}} \text{ and } P_A = \frac{\eta_1 P_0}{\eta_2}$$

and the combining loss is equal to:

$$L_C = 10 \log \frac{P_A}{P_0} = 10 \log \frac{\eta_1}{\eta_2}$$

The efficiencies and calculated losses have been tabulated in Table LII .

TABLE LII . CALCULATED OUTPUT COMBINING LOSSES.

Amplifier Number	800 MHz Calculated Efficiency	800 MHz Measured Efficiency	Combining Loss
7	56.1%	50.1%	.49dB
8	56.9%	51.8%	.41dB
9	56.9%	51.0%	.41dB
10	55.9%	51.5%	.37dB
11	57.1%	50.5%	.53dB

The insertion loss measurements made on the quadrature couplers indicated that 0.25 to 0.3 dB loss could be expected from the quadrature coupler alone. Therefore, the matching circuit variations between the test amplifier and the combined amplifier, plus the effects of the difference port dummy load resistor, are contributing less than 0.2 dB to efficiency degradation of the amplifier.

Some efficiency is lost due to the resistance in the feed chokes. These resistances have been measured and are .45 ohms in

the collector circuit and .05 ohms in the emitter circuit. At 1.07 amps per transistor, the dc power lost in the chokes is:

$$P_L = I^2R = 1.15 \times .5 = ,58 \text{ Watts}$$

Since the typical efficiency at 800 MHz is 55%, eliminating the power lost in the chokes would increase the efficiency to:

$$P_{DC} = \frac{P_O}{\eta} = \frac{18}{.55} = 32.7 \text{ Watts}$$

and,

$$\eta_{CORR} = \frac{18}{32.7 - .58} = \frac{18}{32.1} = 56\%$$

Therefore, some increase in efficiency is possible by reducing the collector dc feed choke resistance, however, the effort required to produce a lower resistance choke (additional masking and plating or a parallel gap welded wire) may not be worth the one per cent increase in efficiency.

2.10 EVALUATION OF THE SB2000 CELL FOR USE IN THE CONTRACT AMPLIFIER

2.10.1 Justification for use of the SB2000 Cell

During the period in which the third and fourth engineering sample amplifiers were built and tested it was obvious that the MW2000 parameter just wasn't working out.

The SB2000 transistor had been developed independently to cover any contingencies found in the MW2000 parameter. It was an interdigitated design using a new proprietary metal system to provide metal migration characteristics better than any available at the time. In addition, the SB2000 incorporated diffused ballast resistors large enough to solve the ruggedness problems of the MW2000. It was, therefore, decided to evaluate the SB2000 performance in the contract amplifier.

2.10.2 SB2000 Preliminary Test Results.

The SB2000 transistor was evaluated and the results were compared with the old MW2000. Performance results are detailed in Tables LIII through LV and show that while the SB2000 gain measurements were lower than desired (7dB, instead of 8dB) device ruggedness was improved and efficiencies were similar.

SB2000 microamps were also installed in earlier produced samples of the contract amplifier. The test results (Tables LVI through LX) verify the test data obtained on the single transistor basis. The output power and efficiency did not change significantly but the gain obtained was approximately one dB lower.

TABLE LIII. TYPICAL PERFORMANCE DATA OBTAINED FROM THE SB2000 CIRCUIT.

f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
600	3.00	1.10	.51	7.8	58.0
700	2.51	1.13	.05	8.5	57.0
800	2.82	1.17	.31	8.0	55.0
900	2.74	1.11	.21	8.2	58.0
1000	3.15	1.18	.20	7.6	54.0

V_{CC} = 28V P_O = 18W

TABLE LIV. TYPICAL PERFORMANCE DATA OBTAINED FROM THE SB2000 CIRCUIT.

f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
600	2.96	1.06	.50	7.8	61.0
700	2.51	1.07	.04	8.6	60.0
800	2.82	1.09	.27	8.0	59.0
900	2.91	1.05	.28	7.9	61.0
1000	3.28	1.10	.21	7.4	58.0

V_{CC} = 28V P_O = 18W

TABLE LV . TYPICAL PERFORMANCE DATA OBTAINED FROM THE SB2000 CIRCUIT.

f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
600	3.14	1.08	.50	7.6	60.0
700	2.65	1.06	.05	8.1	61.0
800	2.93	1.12	.23	7.9	58.0
900	2.94	1.09	.21	7.9	59.0
1000	3.12	1.12	.15	7.6	58.0

V_{CC} = 28V P_O = 18W

TABLE LVI . TYPICAL PERFORMANCE DATA OBTAINED FROM THE INTEGRATED CIRCUIT POWER AMPLIFIER.

f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
600	2.90	1.07	.42	7.9	60.0
700	2.49	1.07	.02	8.6	60.0
800	2.78	1.10	.23	8.1	58.0
900	2.73	1.04	.17	8.2	62.0
1000	3.23	1.09	.38	7.4	59.0

V_{CC} = 28V P_O = 18W

TABLE LVII . TYPICAL PERFORMANCE DATA OBTAINED FROM THE INTEGRATED CIRCUIT POWER AMPLIFIER.

UNIT NO.	f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
22	600	5.92	2.05	.00	7.0	52.2
	650	5.10	2.01	.01	7.7	53.2
	700	4.92	2.06	.06	7.8	52.6
	750	5.04	2.09	.10	7.7	61.2
	800	5.15	2.07	.10	7.7	51.9
	850	5.16	2.04	.10	7.7	52.5
	900	5.18	2.03	.19	7.6	52.9
	950	4.85	1.93	.27	7.9	55.6
	1000	5.37	1.91	.28	7.5	56.1

V_{CC} = 28V P_O = 30W

TABLE LVIII. TYPICAL PERFORMANCE DATA OBTAINED FROM THE INTEGRATED CIRCUIT POWER AMPLIFIER.

UNIT NO.	f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
24	600	6.41	2.02	.00	6.7	53.0
	650	5.21	1.98	.00	7.6	54.1
	700	4.87	2.04	.100	7.9	52.6
	750	5.33	2.08	.00	7.5	51.5
	800	6.11	2.09	.00	6.9	51.2
	850	6.71	2.07	102	6.5	51.9
	900	7.01	2.06	.08	6.3	52.0
	950	6.39	1.94	.10	6.7	55.2
	1000	6.30	1.86	.04	6.8	57.8

V_{CC} = 28V P_O = 30W

TABLE LIX. TYPICAL PERFORMANCE DATA OBTAINED FROM THE INTEGRATED CIRCUIT POWER AMPLIFIER.

UNIT NO.	f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
17	600	5.97	1.99	.01	7.0	53.7
	650	4.88	1.85	.00	7.9	58.0
	700	4.71	1.86	.00	8.0	57.7
	750	4.94	1.95	.02	7.8	55.0
	800	5.24	1.97	.03	7.6	54.3
	850	5.25	1.99	.02	7.6	53.7
	900	5.26	2.06	.02	7.6	52.0
	950	4.66	1.90	.03	8.1	56.2
	1000	5.53	1.96	.01	7.3	54.8

V_{CC} = 28V P_O = 30W

TABLE LX . TYPICAL PERFORMANCE DATA OBTAINED FROM THE INTEGRATED CIRCUIT POWER AMPLIFIER.

UNIT NO.	f (MHz)	P_{IN} WATTS	I_C (ADC)	P_{REF} (W)	G_p dB	EFF. %
21	600	6.00	2.07	.00	7.0	51.8
	650	5.08	1.94	.00	7.7	55.1
	700	5.02	1.97	.01	7.7	54.2
	750	5.70	2.04	.06	7.2	52.7
	800	6.00	2.06	.14	7.0	52.0
	850	6.10	2.06	.12	6.9	52.0
	900	5.78	2.08	.07	7.1	51.5
	950	5.10	1.96	.05	7.7	54.8
	1000	6.10	2.04	.11	6.9	52.7

V_{CC} = 28V P_O = 30W

2.10.3 Design Improvements for Increased Gain.

Three factors were considered during the redesign of the mask for the substrates used in the contract amplifier. First, the input matching network was redesigned for reduced losses. Because the MOS capacitors and the gold bond wires both exhibit more loss than an external microstrip matching section, additional gain could be realized by reducing the internal matching sections and replacing them with microstrip matching sections. In addition, it was found that a more optimum match could be obtained through the accomplishment of this action. The previously designed transistors exhibited input return losses of approximately 10dB, while the new design for the input match was capable of a return loss in the order of 14 dB. Therefore, an additional 0.25 dB of gain was expected due to the improved input return loss alone. The expected increase in gain, due to the reduction in input matching section loss, was 0.7 dB. Secondly, the dc resistance in the distributed emitter feed produced a voltage drop that back biased the transistor, resulting in reduced gain. A 5 mil wire was parallel gap welded to the emitter choke to reduce the voltage drop, but the problem was merely reduced by this procedure. To eliminate the voltage drop, the distributed feed choke was replaced with a lumped inductor with cross sectional area sufficient for the currents found in the emitter return path. A gain increase of 0.5 dB was expected from this change. The distributed dc feedchoke in the collector circuit was replaced with a ferrite bead choke, to essentially eliminate the 0.58 volt drop produced by this choke. This change will produce a 1% increase in efficiency and a calculated increase in gain of 0.1 dB.

All of these changes were expected to increase the module gain by 1.55 dB. The information gained from the preliminary investigation showed that the old circuit and part produced an amplifier with 6.5 to 7.0 dB gain. Therefore, the increased gain

expected from these changes will produce an amplifier module capable of meeting the modified contract specifications of 8 dB.

2.10.4 Design Improvement Verification.

Evaluation of the SB2000 transistor in the final alumina circuit was delayed by the lack of a mask set for the fabrication of the final substrates. The progress of the transistor redesign was, therefore, monitored on teflon fiber glass laminate. A performance baseline was established from the data obtained during the preliminary testing. (Section 2.10.2.)

When the new transistor design was completed, the transistors were evaluated in both an old alumina circuit, modified to the best extent possible, and the teflon fiber glass circuit. The data obtained from the alumina circuit is shown in Tables LXI through LXIII. Although an optimum input match could not be obtained, it should be noted that the performance obtained from the new design is definitely superior to that of the older design. The same transistors were then tested in the teflon fiber glass circuit and the performance obtained is shown in Tables LXIV through LXVI . The better input match produces flatter gain in the teflon fiber glass circuit, but the output match (not the same configuration as the alumina circuit) is worse, resulting in lower efficiency and hence reduced gain for the parts. Data obtained in the teflon fiber glass circuit for a later lot of transistors is shown in Tables LXVII through LXX .

The results from these tests proved that the gain of the new SB2000 transistor is superior to that of the old SB2000 design. Additional gain will be realized when the optimized circuit is used for amplifier construction.

TABLE LXI . NEW SB2000 PERFORMANCE DATA IN OLD CONTRACT TEST FIXTURE.

Transistor #2	f (MHz)	P_{IN} WATTS	P_{REF} (W)	EFF. η %	GAIN dB
	600	2.60	.165	57.0	8.4
	700	2.20	.038	56.0	9.1
	800	2.52	.340	57.0	8.5
	900	2.71	.280	54.0	8.2
	1000	2.15	.125	62.0	9.2

V_{CC} = 28V P_O = 18W

TABLE LXII . NEW SB2000 PERFORMANCE DATA IN OLD CONTRACT TEST FIXTURE.

Transistor #3	f (MHz)	P_{IN} WATTS	P_{REF} (W)	EFF. η %	GAIN dB
	600	2.52	.160	56.0	8.5
	700	2.10	.030	58.0	9.3
	800	2.27	.240	59.0	9.0
	900	2.27	.180	60.0	9.0
	1000	2.14	.147	62.0	9.2

V_{CC} = 28V P_O = 18W

TABLE LXIII. NEW SB2000 PERFORMANCE DATA IN OLD CONTRACT TEST FIXTURE.

Transistor #4	f (MHz)	P_{IN} WATTS	P_{REF} (W)	EFF. η %	GAIN dB
	600	2.65	.108	53.0	8.3
	700	2.28	.064	57.0	9.0
	800	2.48	.310	57.0	8.6
	900	2.51	.155	57.0	8.5
	1000	2.39	.235	61.0	8.8

V_{CC} = 28V P_O = 18W

TABLE LXIV. NEW SB2000 PERFORMANCE DATA IN PRODUCTION TEST FIXTURE.

Transistor #2	f (MHz)	P_{IN} WATTS	P_{REF} (W)	EFF. η %	GAIN dB
	600	2.40	.084	50.0	8.75
	700	1.78	.020	64.0	10.05
	800	2.20	.080	56.0	9.10
	900	2.31	.003	55.0	8.90
	1000	2.20	.060	61.0	9.10

V_{CC} = 28V P_O = 18W

TABLE LXV . NEW SB2000 PERFORMANCE DATA IN PRODUCTION TEST FIXTURE.

Transistor #4	f (MHz)	P_{IN} WATTS	P_{REF} (W)	EFF. η %	GAIN dB
	600	2.35	.082	52.0	8.8
	700	1.86	.012	64.0	9.9
	800	2.30	.048	55.0	9.4
	900	2.39	.056	55.0	8.8
	1000	2.30	.098	58.0	8.8

V_{CC} = 28V P_O = 18W

TABLE LXVI . NEW SB2000 PERFORMANCE DATA IN PRODUCTION TEST FIXTURE.

Transistor #3	f (MHz)	P_{IN} WATTS	P_{REF} (W)	EFF. η %	GAIN dB
	600	2.42	.071	50.0	8.7
	700	1.91	.025	64.0	9.7
	800	2.38	.036	55.0	8.8
	900	2.48	.013	54.0	8.6
	1000	2.35	.018	61.0	8.8

V_{CC} = 28V P_O = 18W

TABLE LXVII . TYPICAL PERFORMANCE DATA OBTAINED FROM PRODUCTION TEST FIXTURE (All Return Losses Less Than -16dB).

Unit #2 .

f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	GAIN dB
600	2.26	1.00	64.0	9.0
700	2.12	1.01	64.0	9.3
800	2.24	1.05	61.0	9.0
900	2.28	1.00	64.0	9.0
1000	2.17	.99	65.0	9.2

V_{CC} = 28V P_O = 18W

TABLE LXVIII. TYPICAL PERFORMANCE DATA OBTAINED FROM PRODUCTION TEST FIXTURE (All Return Losses Less Than -16dB).

Unit #1

f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	GAIN dB
600	2.22	1.01	64.0	9.1
700	2.07	1.02	63.0	9.4
800	2.19	1.06	61.0	9.1
900	2.26	1.02	63.0	9.0
1000	2.12	1.00	64.0	9.3

V_{CC} = 28V P_O = 13W

TABLE LXIX. TYPICAL PERFORMANCE DATA OBTAINED FROM PRODUCTION TEST FIXTURE (All Return Losses Less Than -16dB).

Unit #4

f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	GAIN dB
600	2.31	.99	65.0	8.9
700	2.20	1.02	63.0	9.1
800	2.29	1.06	61.0	9.0
900	2.30	1.02	63.0	8.9
1000	2.22	1.01	64.0	9.1

V_{CC} = 28V P_O = 18W

TABLE LXX . TYPICAL PERFORMANCE DATA OBTAINED FROM PRODUCTION TEST FIXTURE (All Return Losses Less Than -16dB).

Unit #3

f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	GAIN dB
600	2.22	1.02	63.0	9.1
700	2.09	1.02	63.0	9.3
800	2.18	1.05	61.0	9.2
900	2.19	1.01	64.0	9.1
1000	2.05	.99	65.0	9.4

V_{CC} = 28V P_O = 18W

2.11 FIFTH ENGINEERING SAMPLE AMPLIFIERS.

2.11.1 Fifth Engineering Sample Description.

The fifth engineering samples were built to prove the feasibility of producing contract amplifiers using the SB2000 transistor. These samples were built in the housings designed for the first article samples and were fully representative of the performance expected from the first articles except that the housings were not hermetically sealed.

The substrate was redesigned to provide additional gain for margin in meeting the contract specifications of 8 dB. This redesign changed the internal matching network inside the MRA transistor, and the external matching network on the alumina substrate. Because the bond wires and the MOS capacitors used to form the internal matching elements exhibit considerably more loss than the distributed matching elements on the alumina substrate, it was found that a substantial gain increase could be obtained by reducing the internal matching network to one section and increasing the external matching network to two sections. In addition, the distributed dc feedchokes were replaced with lumped feedchokes to reduce the dc voltage drop previously encountered. The design change allowed better realization of the input match, thus producing more gain.

2.11.2 Test Results Fifth Engineering Samples.

Three engineering sample amplifiers were fabricated and tested. The MRA transistors used for fabrication of these amplifiers were selected from the lower end of the gain distribution curve in an attempt to determine the amount of margin for production of the amplifier. The parts used exhibited approximately one half dB less gain than a nominal transistor.

The engineering sample amplifiers were pretuned by connecting in all of the tuning adjustments necessary to achieve the performance required by the contract specifications. The important point is that all three amplifiers were tuned identically and all three amplifiers met the contract requirements with no individual adjustments.

The test results, Tables LXXI through LXXXI , show that the low gain transistors produce a module meeting the contract requirements. All of the remaining electrical parameters of the engineering sample amplifiers are well within the contract specifications as defined in SCS 409A including the VSWR survival requirements. It was expected that the amplifier can be produced in production quantities with relative ease and freedom from precise tuning and adjusting of the alunina circuitry. A mask revision was generated to allow fabrication of substrates to this configuration without the tuning adjustments required by the previous mask set.

TABLE LXXI . ENGINEERING TEST SAMPLE AMPLIFIER #1 PERFORMANCE AT T = 20°C.

#1	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.65	2.06	52.0	8.1
	650	4.30	2.04	52.0	8.4
	700	4.20	2.02	53.0	8.5
	750	4.30	2.00	54.0	8.4
	800	4.25	1.98	54.0	8.5
	850	4.15	1.95	54.0	8.6
	900	4.10	1.94	54.0	8.6
	950	4.10	1.93	55.0	8.6
	1000	4.35	1.96	54.0	8.4

V_{CC} = 28V P_O = 30W L_R (dB) = >20
T_C = 25°C

TABLE LXXII . ENGINEERING TEST SAMPLE AMPLIFIER #1, PERFORMANCE AFTER 3:1 VSWR, 30V OVERVOLTAGE.

#1	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.70	2.06	52.0	8.1
	650	4.30	2.05	52.0	8.4
	700	4.15	2.01	53.0	8.5
	750	4.30	2.00	54.0	8.4
	800	4.25	1.98	54.0	8.5
	850	4.20	1.95	54.0	8.6
	900	4.10	1.94	54.0	8.6
	950	4.05	1.94	54.0	8.6
	1000	4.30	1.96	54.0	8.4

V_{CC} = 28V P_O = 30W L_R (dB) = >20
T_C = 25°C

TABLE LXXIII. ENGINEERING TEST SAMPLE AMPLIFIER #1, PERFORMANCE AT T = 80°C.

#1	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.35	2.09	51.0	8.4
	650	4.10	2.08	51.0	8.6
	700	4.00	2.07	52.0	8.7
	750	4.10	2.06	52.0	8.6
	800	4.05	2.02	53.0	8.7
	850	3.95	1.98	54.0	8.8
	900	4.00	2.00	54.0	8.7
	950	4.05	2.00	54.0	8.7
	1000	4.40	2.08	51.0	8.3

V_{CC} = 28W P_O = 30W L_R (dB) = >20
T_C = 80°C

TABLE LXXIV. ENGINEERING TEST SAMPLE AMPLIFIER #2, PERFORMANCE AT T = 20°C.

#2	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.45	1.97	54.0	8.3
	650	3.95	1.93	56.0	8.8
	700	3.65	1.91	56.0	9.1
	750	3.70	1.93	56.0	9.1
	800	3.75	1.94	55.0	9.0
	850	3.75	1.91	56.0	9.0
	900	3.75	1.93	56.0	9.0
	950	3.90	1.94	56.0	8.9
	1000	4.05	1.98	54.0	8.7

V_{CC} = 28V P_O = 30W L_R (dB) = >20
T_C = 25°C

TABLE LXXV . ENGINEERING TEST SAMPLE AMPLIFIER #2, PERFORMANCE AFTER 3:1 VSWR, 30V OVERVOLTAGE.

#2	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.50	1.96	54.0	8.3
	650	4.00	1.93	56.0	8.8
	700	3.60	1.92	56.0	9.1
	750	3.70	1.93	56.0	9.1
	800	3.75	1.93	56.0	9.0
	850	3.75	1.91	56.0	9.0
	900	3.75	1.94	55.0	8.9
	950	3.85	1.94	56.0	8.9
	1000	4.10	1.97	54.0	8.7

V_{CC} = 28V P_O = 30W T_C = 25°C L_R(dB) = >20

TABLE LXXVI . ENGINEERING TEST SAMPLE AMPLIFIER #2, PERFORMANCE AT T = 80°C.

#2	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.20	1.97	54.0	8.5
	650	3.75	1.96	54.0	9.0
	700	3.50	1.95	54.0	9.3
	750	3.55	2.00	54.0	9.3
	800	3.60	1.98	54.0	9.2
	850	3.60	1.96	54.0	9.2
	900	3.70	2.00	54.0	9.1
	950	3.85	2.02	53.0	8.9
	1000	4.20	2.10	51.0	8.5

V_{CC} = 28V P_O = 30W T_C = 80°C L_R (dB) = >20

TABLE LXXVII . ENGINEERING TEST SAMPLE AMPLIFIER #3, PERFORMANCE AT T = 20°C.

#3	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.65	1.98	54.0	8.1
	650	4.40	1.99	54.0	8.3
	700	4.20	1.96	54.0	8.5
	750	4.20	1.93	56.0	8.5
	800	4.20	1.92	56.0	8.5
	850	4.25	1.92	56.0	8.5
	900	4.35	1.91	56.0	8.4
	950	4.50	1.90	56.0	8.2
	1000	4.70	1.93	56.0	8.05

V_{CC} = 28V P_O = 30W L_R (dB) = >20
T_C = 25°C

TABLE LXXIII. ENGINEERING TEST SAMPLE AMPLIFIER #3, PERFORMANCE AFTER 3:1 VSWR, 30V OVERVOLTAGE.

#3	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_p dB
	600	4.72	1.96	54.0	8.02
	650	4.30	1.92	56.0	8.4
	700	4.05	1.89	57.0	8.7
	750	4.15	1.94	55.0	8.6
	800	4.25	1.94	55.0	8.5
	850	4.20	1.93	56.0	8.5
	900	4.45	1.98	54.0	8.3
	950	4.70	1.95	55.0	8.05
	1000	4.70	1.92	56.0	8.05

V_{CC} = 28V P_O = 30W L_R (dB) = >20
T_C = 25°C

TABLE LXXIX. ENGINEERING TEST SAMPLE AMPLIFIER #3, PERFORMANCE AT T = 80°C.

#3	f (MHz)	P_{IN} WATTS	I_C (ADC)	EFF. η %	G_P dB
	600	4.35	2.00	54.0	8.4
	650	3.90	1.94	55.0	8.9
	700	3.75	1.93	55.0	9.0
	750	3.90	1.98	54.0	8.9
	800	4.05	1.99	55.0	8.7
	850	4.00	1.98	54.0	8.8
	900	4.25	2.03	53.0	8.5
	950	4.45	2.00	54.0	8.3
	1000	4.20	2.11	51.0	8.05

V_{CC} = 28V P_O = 30W T_C = 80°C L_R (dB) = >20

TABLE LXXX . IN-OUT PHASE ANGLES FOR ENGINEERING TEST SAMPLE AMPLIFIERS.

f(MHz)	#1	#2	#3
600	+176	+168	+160
650	+ 88	+ 80	+ 71
700	- 6	- 16	- 21
750	-100	-110	-116
800	+166	+155	+151
850	+ 68	+ 58	+ 53
900	- 32	- 42	- 46
950	-136	-143	-145
1000	+106	+110	+ 93

V_{CC} = 28V P_O = 30W L_R (dB) = >20

TABLE LXXXI . PHASE VARIATIONS FOR ENGINEERING TEST SAMPLE AMPLIFIERS.

f (MHz)	θ Max (Degrees)	θ Min (Degrees)	Δ θ (Degrees)
600	176	160	16
650	88	71	17
700	-6	-21	15
750	-100	-116	16
800	166	151	15
850	68	53	15
900	-32	-46	14
950	-136	-145	9
1000	106	93	13

2.12 FIRST ARTICLE SAMPLES

2.12.1 First Article Description.

The first article amplifiers were intended to show the complete characteristics of the final amplifier design in significant quantities. These amplifiers were fabricated using the production techniques intended for use in the production run. The completed amplifiers were subjected to qualification testing at the same levels as slated for the production amplifiers.

2.12.2 First Article Mechanical Design.

The housings for the first article samples were machined from a solid block of aluminum. All of the machining was completed except for the tapped holes for kovar and micro-amp mounting. The area under the micro-amp transistor flanges was not finish machined. The housing and cover were then masked and nickle plated to provide solderable surfaces. The masking provided aluminum to aluminum contact in the seal area for welding purposes. Figures 48 and 49 show the machining details of the housing and cover. After plating and mask stripping, the final machining is completed. This involves the tapping of the holes and final machining of the transistor mounting surface.

The Kovar plates (Figure 50) for substrate mounting were machined, nickle plated and gold flashed for solderability. Fabrication of the ground clips (Figure 51) by forming brass shim stock in a bending fixture and machining the pinch-off tube (Figure 52) completed the piece part fabrication.

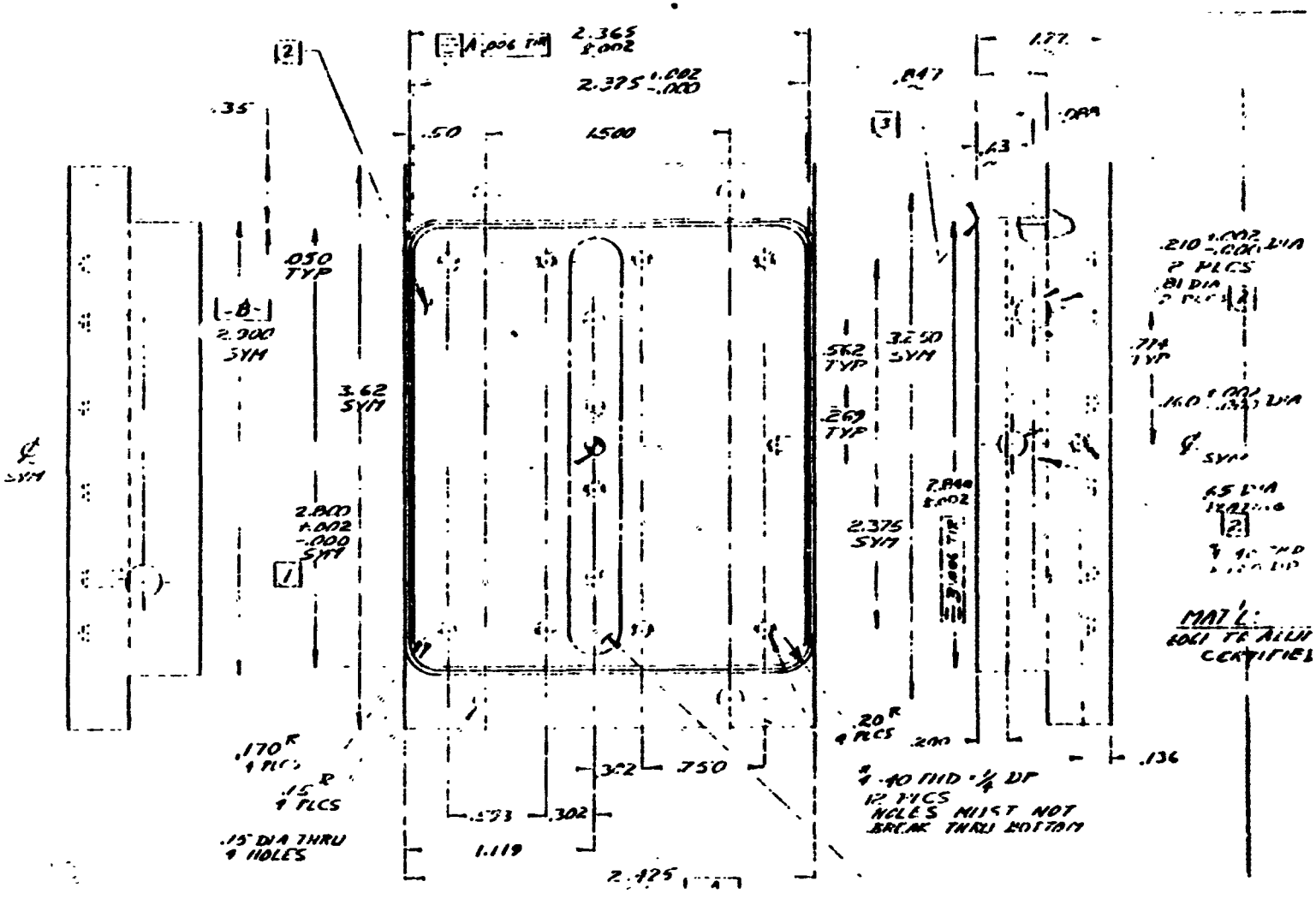


Figure 48. First Article Housing Machine Drawing.

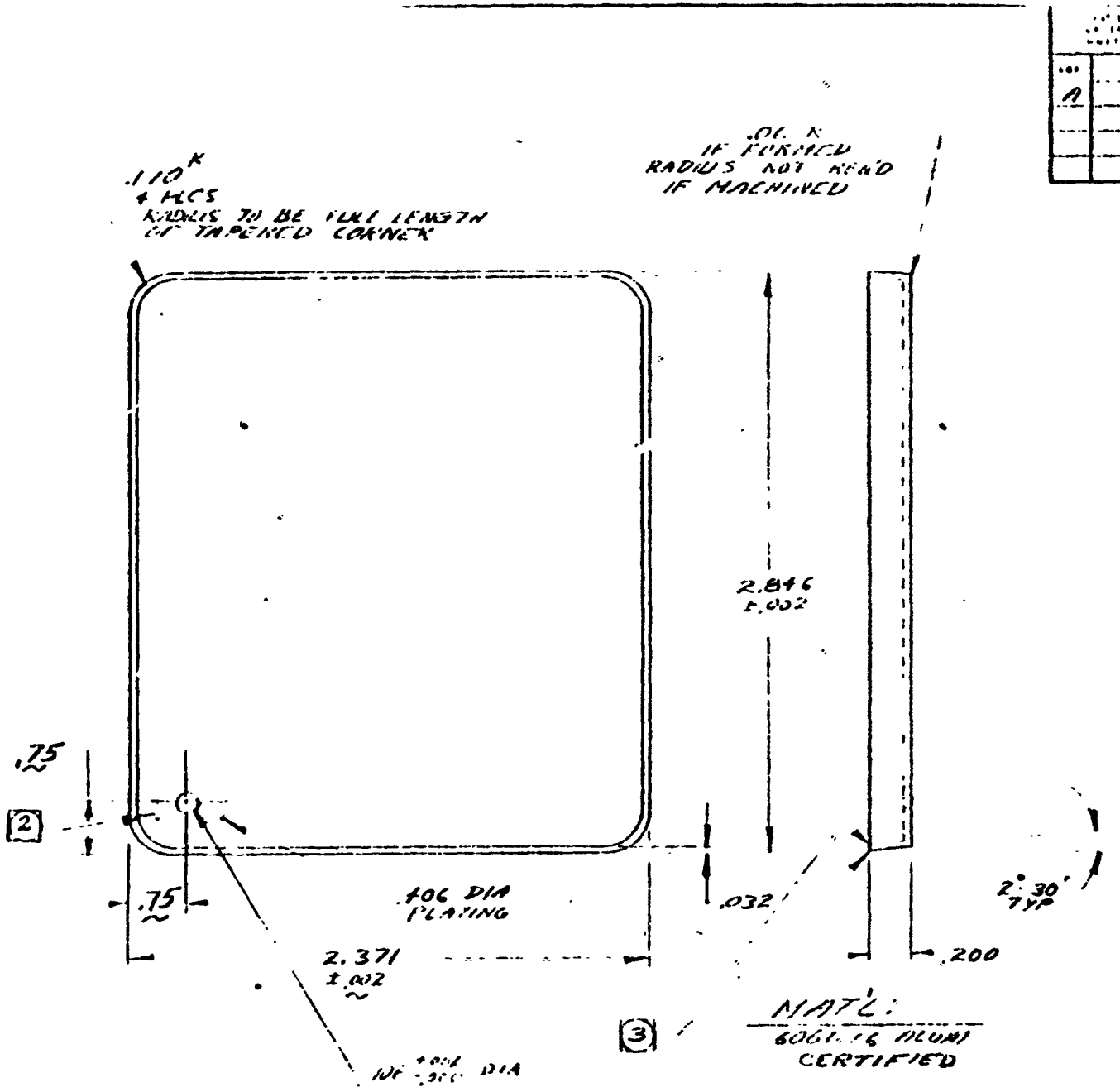


Figure 49. First Article Cover Machine Drawing.

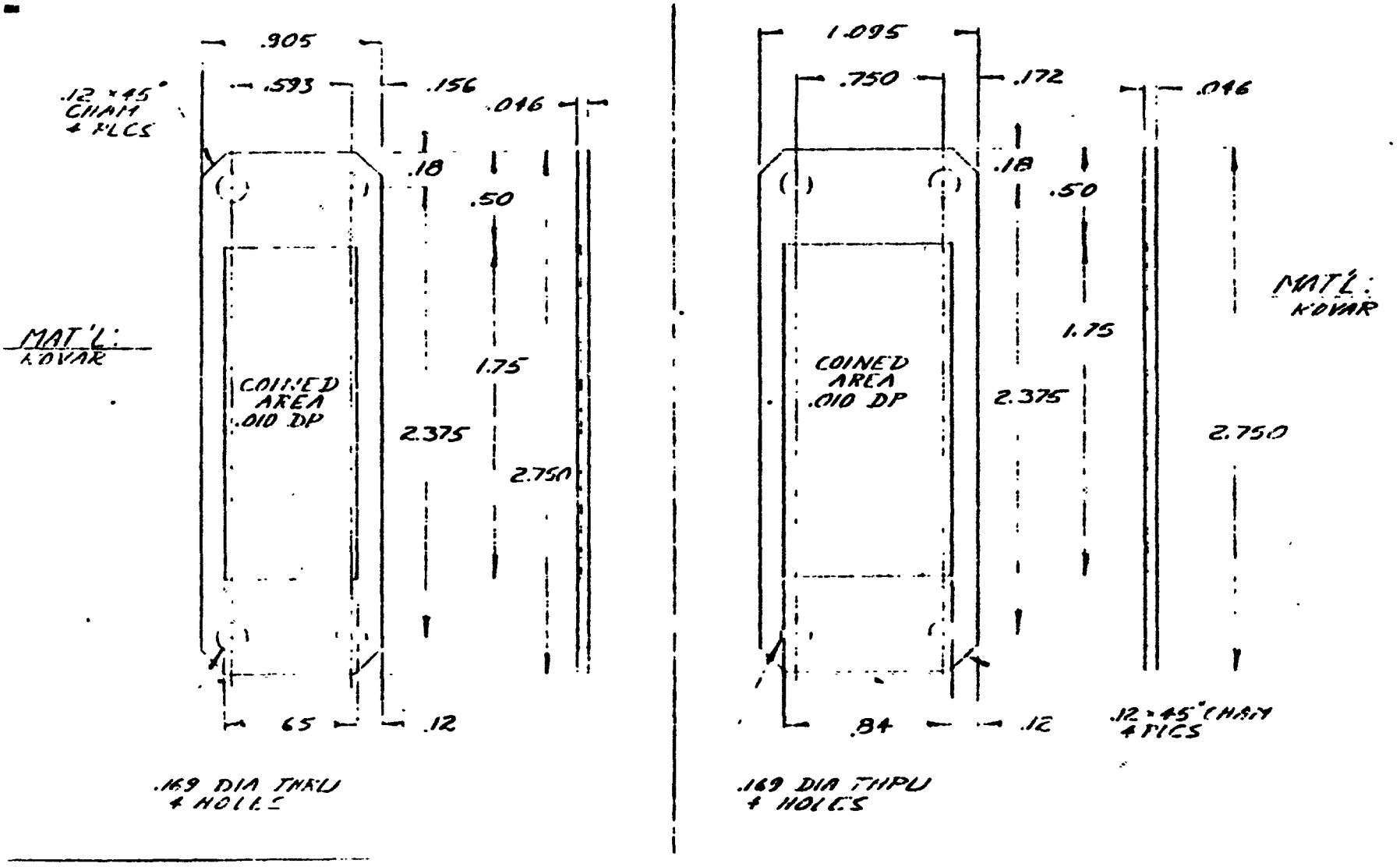


Figure 50. First Article Kovar Machine Drawing.

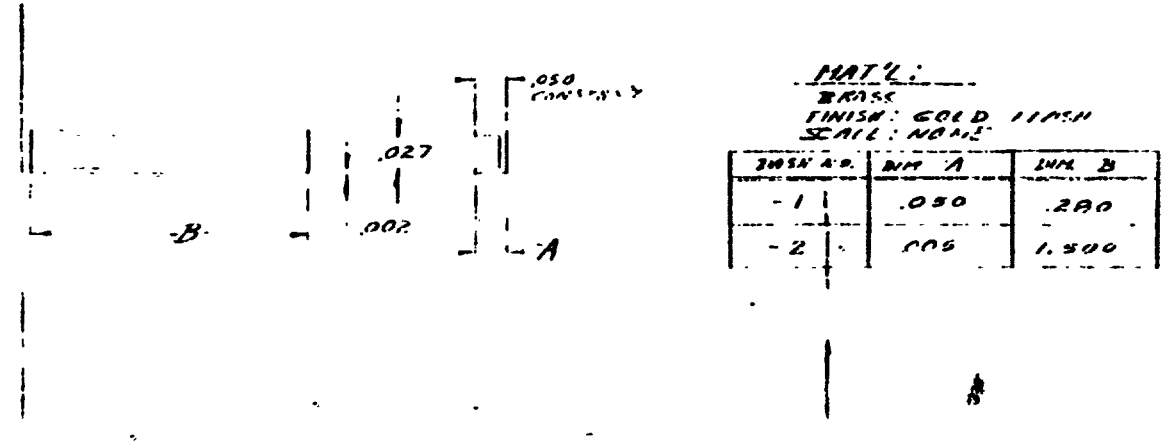
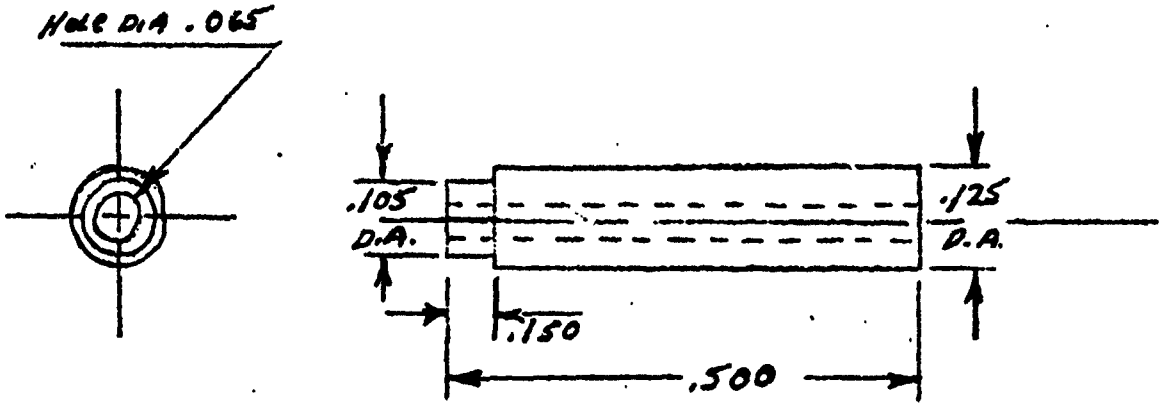


Figure 51. First Article Ground Clip Drawing.

LET.	REVISIONS	E.C.N. NO.	DRAWN BY	APPR	DATE



MAT'L: FULL ANNEALED
DEAD SOFT COPPER

UNLESS OTHERWISE SPECIFIED
TOLERANCES ON
XXX ± .005
XX ± 0.5
ANGULAR ± 0°30'

SCALE

DRAWN | CHECKED | APPROV

PINCH OFF TUBE FOR PA - 1120

TRW SEMICONDUCTOR DIV.

DWG. NO. 80F00029

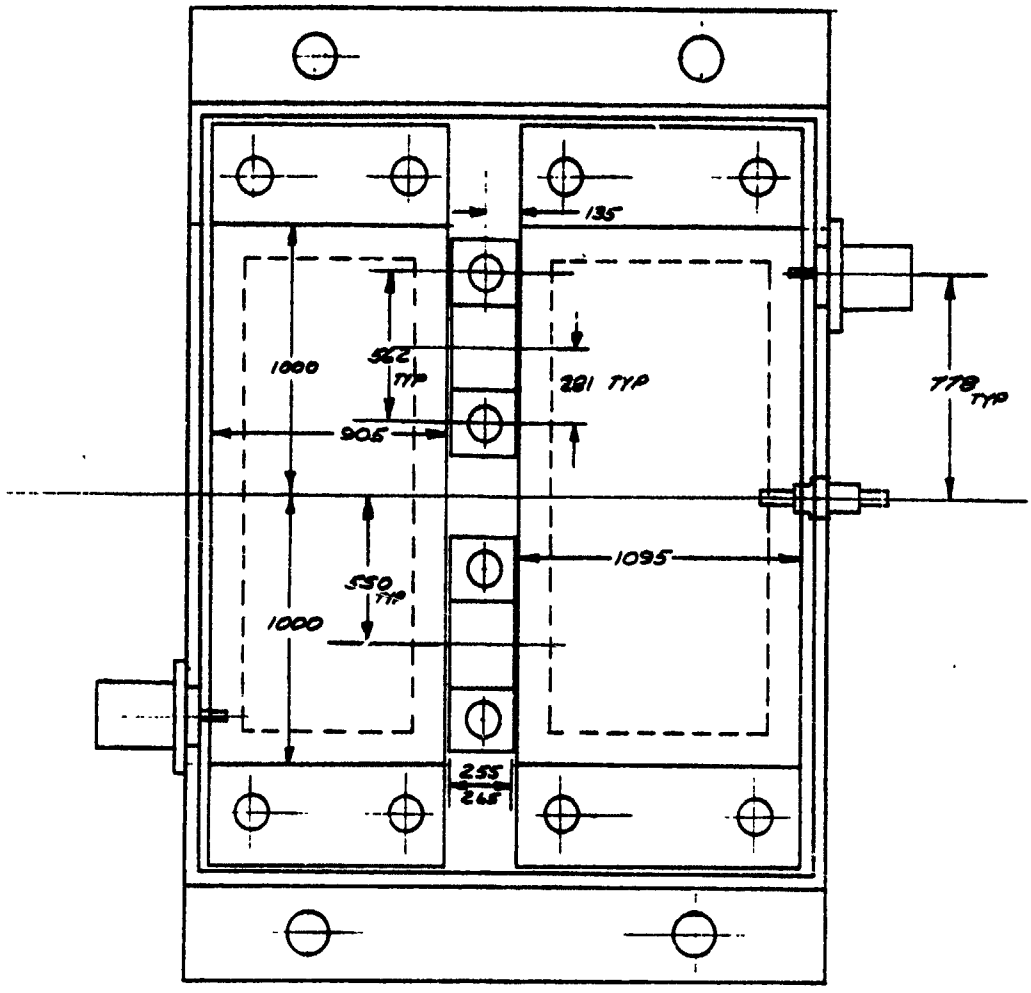
Figure 52. First Article Pinch Off Tube.

2.12.3 Final Assembly.

Final assembly is initiated by soldering the kovar plates to the housing with 95% tin 5% lead solder. While the solder is molten, the hold down screws are installed, insuring complete solder flow and dimensional accuracy. Next the input and output connectors and the B+ feed thru were installed using 60% tin 40% lead solder. At this point a gross leak test was performed by using a clamped on lid for pressurization. Twenty-five pounds per square inch internal pressure provided good leak detection sensitivity. The input and output substrates were installed and soldered to the kovar plates with indialloy #2 solder. Installation of the micro-amp transistors with a thin coating of Wakefield thermal grease applied to the interface completed the mechanical assembly. The remaining step was that of soldering down the connector tabs, the transistor leads and installing the B+ wiring straps. Figure 53 is a sketch of the amplifier assembly.

2.12.4 Group A Test Results First Article Amplifiers.

The Group A testing shows that the first article amplifiers meet all of the specifications delineated in SCS-409A. Tables LXXXII through XCVI show the point by point readings taken on each individual amplifier, while Table XCVII lists the highest and lowest performance obtained from all amplifiers along with the delta performance. All of the gain and phase windows were utilized as a minimum of individual amplifier tuning was performed. Less of the gain and phase windows could have been used if more individual tuning had been performed. The batch processing concept of the contract dictated that minimum tuning was the preferred condition.



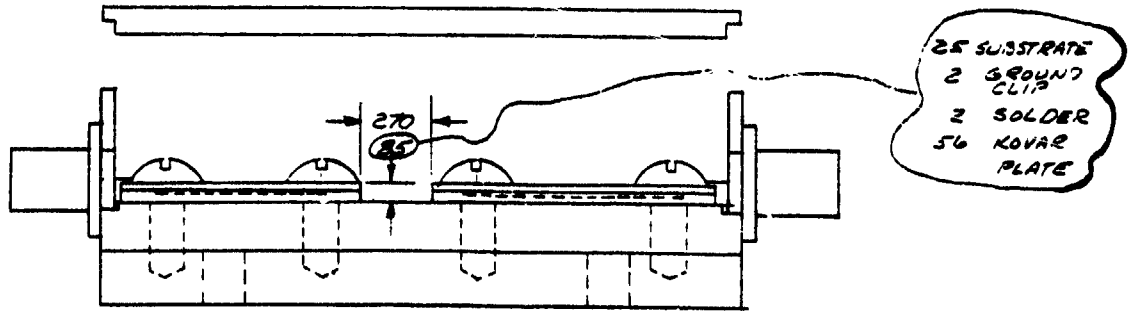


Figure 53. 600-1000 MHz 30W First Article Amplifier Assembly Sketch. (Scale 1x All Dimensions in Mils.)

TABLE LXXXII . UNIT #24 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.72	2.02	9.1	53	- 43
650	3.74	2.03	9.0	53	-115
700	3.70	1.99	9.1	54	164
750	3.82	1.97	9.0	54	84
800	3.86	1.96	8.9	55	3
850	3.85	1.98	8.9	54	- 77
900	3.87	1.98	8.9	54	-159
950	3.98	2.00	8.8	54	118
1000	3.96	1.96	8.8	55	33

TABLE LXXXIII. UNIT #26 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 14 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	4.35	2.13	8.4	50	- 40
650	4.01	2.09	8.7	51	-113
700	3.85	2.02	8.9	53	167
750	3.99	2.00	8.8	54	86
800	4.04	1.98	8.7	54	5
850	4.04	1.99	8.7	54	- 75
900	4.08	1.99	8.7	54	-156
950	4.27	2.01	8.4	53	122
1000	4.39	1.96	8.3	55	37

TABLE LXXXIV. UNIT #27 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.81	2.03	9.0	53	- 45
650	3.74	2.02	9.0	53	-117
700	3.65	1.96	9.1	55	162
750	3.67	1.91	9.1	56	82
800	3.67	1.90	9.1	56	1
850	3.60	1.91	9.2	56	- 80
900	3.55	1.91	9.3	56	-163
950	3.72	1.98	9.1	54	111
1000	3.77	2.00	9.0	54	20

TABLE LXXXV . UNIT #28 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 16 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	4.09	2.10	8.6	51	- 36
650	3.92	2.13	8.8	50	-111
700	3.83	2.12	8.9	51	167
750	3.87	2.08	8.9	52	85
800	3.80	2.05	9.0	52	4
850	3.85	2.05	8.9	52	- 81
900	4.00	2.04	8.7	53	-162
950	4.26	2.06	8.5	52	113
1000	4.10	1.98	8.6	54	17

TABLE LXXXVI . UNIT #29 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	4.00	2.06	8.8	52	- 40
650	3.79	2.03	9.0	53	-115
700	3.64	1.97	9.1	54	164
750	3.66	1.94	9.1	55	82
800	3.61	1.92	9.2	56	1
850	3.56	1.92	9.3	56	- 82
900	3.64	1.93	9.2	56	-165
950	3.90	1.98	8.9	59	110
1000	4.01	1.94	8.7	55	21

TABLE LXXXVII . UNIT #30 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.83	2.06	8.9	52	- 37
650	3.60	2.01	9.2	53	-114
700	3.52	1.98	9.3	54	164
750	3.68	2.00	9.1	54	83
800	3.71	2.02	9.1	53	3
850	3.70	2.05	9.1	52	- 79
900	3.86	2.04	8.9	53	-159
950	3.90	1.93	8.9	56	121
1000	3.74	1.82	9.0	59	34

TABLE LXXXVIII.UNIT #31 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.84	2.00	8.9	54	- 40
650	3.62	1.96	9.2	55	-112
700	3.46	1.90	9.4	56	166
750	3.51	1.88	9.3	57	84
800	3.48	1.87	9.4	54	3
850	3.41	1.88	9.4	57	- 80
900	3.60	1.94	9.2	55	-163
950	3.75	1.91	9.0	56	116
1000	3.62	1.82	9.2	59	29

TABLE LXXXIX. UNIT #33 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.65	2.00	9.1	54	- 47
650	3.60	2.03	9.2	53	-119
700	3.52	1.98	9.3	54	162
750	3.61	1.94	9.2	55	80
800	3.65	1.94	9.1	55	0
850	3.68	1.97	9.1	54	- 82
900	3.74	1.97	9.0	54	-164
950	3.78	1.93	9.0	56	114
1000	3.62	1.84	9.2	58	23

TABLE XC . UNIT #34 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.83	1.93	8.9	56	- 32
650	3.63	1.92	9.2	56	-108
700	3.50	1.88	9.3	57	169
750	3.66	1.89	9.1	57	86
800	3.73	1.86	9.0	58	7
850	3.57	1.82	9.2	59	- 75
900	3.61	1.83	9.2	58	-157
950	3.90	1.88	8.8	57	120
1000	3.91	1.86	8.8	58	29

TABLE XCI . UNIT #35 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 19 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.85	2.02	8.9	53	- 34
650	3.74	1.99	9.0	54	-110
700	3.56	1.93	9.2	56	168
750	3.67	1.92	9.1	56	86
800	3.69	1.88	9.1	57	6
850	3.45	1.83	9.4	58	- 77
900	3.45	1.82	9.4	59	-161
950	3.62	1.86	9.2	58	117
1000	3.55	1.81	9.3	59	28

TABLE XCII. UNIT #36 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.69	2.00	9.1	54	- 41
650	3.56	1.96	9.2	55	-114
700	3.41	1.87	9.4	57	165
750	3.35	1.84	9.5	58	83
800	3.42	1.86	9.4	58	0
850	3.45	1.96	9.4	55	- 86
900	3.56	1.98	9.2	54	-169
950	3.58	1.92	9.2	56	112
1000	3.49	1.86	9.3	58	26

TABLE XCIII. UNIT #37 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.84	2.04	8.9	53	- 33
650	3.50	1.95	9.2	55	-113
700	3.52	1.91	9.3	56	163
750	3.20	1.89	9.1	56	82
800	3.70	1.86	9.1	58	8
850	3.56	1.84	9.2	58	- 80
900	3.50	1.84	9.3	58	-164
950	3.74	1.90	9.0	56	110
1000	3.80	1.86	9.0	58	18

TABLE XCIV. UNIT #38 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 23 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.90	2.15	8.9	50	- 34
650	3.60	2.04	9.2	53	-113
700	3.60	2.01	9.2	53	167
750	3.80	2.01	9.0	53	83
800	3.70	1.98	9.1	54	5
850	3.60	1.97	9.2	54	- 83
900	3.60	1.98	9.2	54	-163
950	4.00	2.07	8.7	52	115
1000	4.00	2.07	8.7	52	22

TABLE XCV . UNIT #39 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.50	2.09	9.3	51	- 37
650	3.40	2.09	9.5	51	-115
700	3.25	2.03	9.7	53	164
750	3.38	2.03	9.5	53	83
800	3.40	2.05	9.5	52	2
850	3.30	2.09	9.6	51	- 79
900	3.45	2.13	9.4	50	-164
950	3.40	2.05	9.5	52	112
1000	3.50	1.92	9.3	56	24

TABLE XCVI . UNIT #40 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30 WATTS, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	4.01	2.04	8.7	53	- 31
650	3.92	2.04	8.8	53	-110
700	3.96	2.02	8.8	53	167
750	4.20	2.03	8.5	53	85
800	4.23	1.99	8.5	54	7
850	4.02	1.93	8.7	56	- 74
900	3.92	1.85	8.8	58	-158
950	3.94	1.82	8.8	59	119
1000	3.84	1.76	8.9	60	29

TABLE XCVII . SUMMARY OF R.F. PERFORMANCE OF FIRST ARTICLE AMPLIFIERS.

	GAIN (dB)			PHASE (DEGREES)			EFFICIENCY (%)		
f MHz	MIN	MAX	DELTA	MIN	MAX	DELTA	MIN	MAX	DELTA
600	8.4	9.3	0.9	- 47	- 31	16	50	56	6
650	8.7	9.5	0.8	-119	-108	11	50	56	6
700	8.8	9.7	0.9	+162	+169	7	51	57	6
750	8.5	9.5	1.0	+ 80	+ 86	6	52	58	6
800	8.5	9.5	1.0	0	+ 8	8	52	58	6
850	8.7	9.6	0.9	- 86	- 74	12	51	59	8
900	8.7	9.4	0.7	-169	-156	13	50	59	9
950	8.4	9.5	0.9	+110	+122	12	52	59	7
1000	8.3	9.3	1.0	+ 17	+ 37	20	52	60	8

2.12.5 Group B Test Results, First Article Amplifiers.

2.12.5.1 Vibration, Shock and Acceleration Testing

Three of the first article amplifiers (serial numbers 33, 35, and 40) were vibrated in accordance with mil standard 883A, Method 2007, condition A. This test provides a sinusoidal vibration of 20 g limited to 0.06 inches of double amplitude from 20 to 2000 hertz. The duration of the sweep is four minutes and each axis is swept four times thur producing a total test time of 48 minutes. Tables XCVIII, XCIX and C show the pre-test baseline data for the 3 units. Tables CI , CII , and CIII show the post vibration data for the same amplifiers. No significant performance changes were noted after vibration testing.

The same three amplifiers were then subjected to mechanical shock in accordance with mil standard 883A, method 2002, condition A. This test requires that the unit under test be subjected to a shock level of 500 g for a pulse duration of 1 millisecond in each of the six axes. Tables CIV, CV and CVI show the post shock data for the amplifiers. No significant performance changes were noted after shock testing.

The same three amplifiers were subjected to linear acceleration in accordance with mil standard 883, method 2001, condition A. This provides 5000 g acceleration in each of the six axes. A fourth amplifier was also subjected to this test because the apparatus used required that the amplifiers be mounted in pairs for balance of the test machine. One amplifier failed during acceleration in the Y1 axis. The plating separated from the aluminum housing which cracked the output alumina substrate. Subsequent tests were run on extra housings to determine whether the problem was isolated to this particular unit or was more general in nature. In every case the solder broke loose before any damage was done to the plating. Another amplifier (serial number 44) was fabricated and subjected to linear acceleration along with an amplifier for

TABLE XCVIII. UNIT #33 PRE VIBRATION, SHOCK, AND ACCELERATION TEST R.F. DATA
$T = 80°C$, $P_{OUTPUT} = 30W$, $V_{CC} = 28V$, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.65	2.00	9.1	54
650	3.60	2.03	9.2	53
700	3.52	1.98	9.3	54
750	3.61	1.94	9.1	55
800	3.65	1.94	9.1	55
850	3.68	1.97	9.1	54
900	3.74	1.97	9.0	54
950	3.78	1.93	9.0	56
1000	3.62	1.84	9.2	58

TABLE XCIV. UNIT #35 PRE VIBRATION, SHOCK, AND ACCELERATION TEST R.F. DATA
$T = 80°C$, $P_{OUTPUT} = 30W$, $V_{CC} = 28V$, RETURN LOSS = > 19 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.85	2.02	8.9	53
650	3.74	1.99	9.0	54
700	3.56	1.93	9.2	56
750	3.67	1.92	9.1	56
800	3.69	1.88	9.1	57
850	3.45	1.83	9.4	58
900	3.45	1.82	9.4	59
950	3.62	1.86	9.2	58
1000	3.55	1.81	9.3	59

TABLE C . UNIT #40 PRE VIBRATION, SHOCK, AND ACCELERATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.01	2.04	8.7	53
650	3.92	2.04	8.8	53
700	3.96	2.02	8.8	53
750	4.20	2.03	8.5	53
800	4.23	1.99	8.5	54
850	4.02	1.93	8.7	56
900	3.72	1.85	8.8	58
950	3.94	1.82	8.8	59
1000	3.84	1.76	8.9	60

TABLE CI . UNIT #33 POST VIBRATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.67	2.00	9.1	54
650	3.62	2.02	9.2	53
700	3.53	1.98	9.2	54
750	3.65	1.94	9.1	55
800	3.65	1.95	9.1	55
850	3.67	1.97	9.1	54
900	3.70	1.97	9.1	54
950	3.78	1.94	9.0	55
1000	3.61	1.84	9.2	58

TABLE CII . UNIT #35 POST VIBRATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.86	2.00	8.9	54
650	3.76	1.98	9.0	54
700	3.60	1.92	9.2	56
750	3.70	1.91	9.1	56
800	3.70	1.88	9.1	57
850	3.48	1.82	9.4	59
900	3.45	1.82	9.4	59
950	3.65	1.85	9.1	58
1000	3.58	1.80	9.2	60

TABLE CIII. UNIT #40 POST VIBRATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.05	2.04	8.7	53
650	3.95	2.02	8.8	53
700	4.00	2.00	8.7	54
750	4.25	2.05	8.5	52
800	4.27	1.98	8.5	54
850	4.05	1.91	8.7	56
900	3.95	1.84	8.8	58
950	3.96	1.81	8.8	59
1000	3.86	1.75	8.9	61

TABLE CIV. UNIT #33 POST SHOCK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.68	2.02	9.1	53
650	3.62	2.04	9.2	53
700	3.60	1.99	9.2	54
750	3.65	1.95	9.1	55
800	3.66	1.95	9.1	55
850	3.68	1.98	9.1	54
900	3.74	1.97	9.0	54
950	3.78	1.94	9.0	55
1000	3.62	1.84	9.2	58

TABLE CV . UNIT #35 POST SHOCK TEST R.F. DATA T + 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.85	2.02	8.9	53
650	3.77	1.99	9.0	54
700	3.60	1.94	9.2	55
750	3.70	1.93	9.1	56
800	3.69	1.89	9.1	57
850	3.47	1.84	9.4	58
900	3.45	1.84	9.4	58
950	3.68	1.87	9.1	57
1000	3.58	1.82	9.2	59

TABLE CVI . UNIT #40 POST SHOCK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.02	2.04	8.7	53
650	3.9[illegible]	2.02	8.8	53
700	4.00	2.02	8.8	53
750	4.22	2.02	8.5	53
800	4.25	1.9[illegible]	8.5	54
850	4.04	1.91	8.7	56
900	3.92	1.85	8.8	58
950	3.94	1.81	8.8	59
1000	3.84	1.75	8.9	61

balance of the accelerator. Both units met the acceleration requirements. Since a total of five amplifiers passed the acceleration test, and the plating peel tests performed on the extra housings indicated that they were free from this problem, the failure was judged to be an isolated failure and not common to all the fabricated amplifiers. Tables CVII and CVIII show the post acceleration data for the two remaining amplifiers that survived linear acceleration. Tables CIX and CX show the pre and post test data for amplifier no. 44. No significant electrical changes were noted after linear acceleration testing.

2.12.5.2 High Temperature Storage.

Two of the first article amplifiers were subjected to a 1000 hour high temperature storage test at 100°C per Mil-Std-883, Method 1008. After the 1000 hour mark the amplifiers (#31 and #34) were electrically tested and the pre test and post test results were compared. Tables CXI through CXIV contain the electrical test data. Comparing the pre test and post test R.F. data reveals no significant changes in performance due to high temperature storage.

2.12.5.3 Steady State Life Testing.

Two of the first article amplifiers (#24 and #27) were subjected to steady state life testing. A block diagram of the steady state and intermittent (See Section 2.12.5.4) life test setup is shown in Figure 54. The steady state testing was done in accordance with Mil-Std-883, Method 1005, Condition B. The steady state life test conditions were: Power output = 30 watts, V_{CC} = 28 VDC, T = 80°C., F = 960 MHz, and test duration = 1000 hours. The pre test R.F. data for the two amplifiers is shown in Tables CXV and CXVII , and after 1000 hours of testing, R. F. data was taken and is shown in Tables CXVI and CXVIII. A comparison of the pre test and post test R.F. data reveals no significant changes in performance.

TABLE CVII . UNIT #33 POST ACCELERATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	CAIN (dB)	η (%)
600	3.73	2.08	9.1	52
650	3.62	2.11	9.2	51
700	3.53	2.04	9.3	53
750	3.62	2.01	9.2	53
800	3.59	2.00	9.2	54
850	3.60	2.02	9.2	53
900	3.64	2.02	9.2	53
950	3.70	1.99	9.1	54
1000	3.49	1.92	9.3	56

TABLE CVIII.UNIT #35 POST ACCELERATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 19 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.92	2.10	8.8	51
650	3.79	2.07	9.0	52
700	3.61	2.00	9.2	54
750	3.68	1.99	9.1	54
800	3.71	1.96	9.1	55
850	3.50	1.92	9.3	56
900	3.46	1.94	9.4	55
950	3.58	1.92	9.2	56
1000	3.55	1.97	9.3	54

TABLE CIX. UNIT #44 PRE ACCELERATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.68	2.02	9.1	53
650	3.52	2.03	9.3	53
700	3.50	2.00	9.3	54
750	3.51	2.01	9.3	53
800	3.72	2.04	9.1	53
850	3.77	2.02	9.0	53
900	3.67	1.91	9.1	54
950	3.66	1.92	9.1	56
1000	3.50	1.86	9.1	58

TABLE CX . UNIT #44 POST ACCELERATION TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 19 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.68	2.04	9.1	53
650	3.52	2.05	9.3	52
700	3.50	2.01	9.3	53
750	3.51	2.03	9.3	53
800	3.72	2.07	9.1	52
85C	3.66	2.08	9.1	52
900	3.67	2.02	9.1	53
950	3.66	1.95	9.1	55
1000	3.50	1.90	9.3	56

TABLE CXI . UNIT #31 PRE HIGH TEMPERATURE STORAGE TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.84	2.00	8.9	54
650	3.62	1.96	9.2	55
700	3.46	1.90	9.4	56
750	3.51	1.88	9.3	57
800	3.48	1.87	9.4	54
850	3.41	1.88	9.4	57
900	3.60	1.94	9.2	55
950	3.75	1.91	9.0	56
1000	3.62	1.82	9.2	59

TABLE CXII . UNIT #31 POST HIGH TEMPERATURE STORAGE TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.84	2.06	8.9	52
650	3.52	2.04	9.3	53
700	3.35	1.96	9.5	55
750	3.28	1.94	9.6	55
800	3.28	1.94	9.6	55
850	3.26	1.98	9.6	54
900	3.50	2.05	9.3	52
950	3.57	1.98	9.2	54
1000	3.40	1.88	9.5	57

TABLE CXIII. UNIT #34 PRE HIGH TEMPERATURE STORAGE TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.83	1.93	8.9	56
650	3.63	1.92	9.2	56
700	3.50	1.88	9.3	57
750	3.66	1.89	9.1	57
800	3.73	1.86	9.0	58
850	3.57	1.82	9.2	59
900	3.61	1.83	9.2	58
950	3.90	1.88	8.8	57
1000	3.91	1.86	8.8	58

TABLE CXIV. UNIT #34 POST HIGH TEMPERATURE STORAGE TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.83	2.02	8.9	53
650	3.58	2.00	9.2	54
700	3.70	1.95	9.3	55
750	3.50	1.94	9.3	55
800	3.54	1.92	9.3	56
850	3.54	1.92	9.3	56
900	3.61	1.94	9.2	55
950	3.79	1.93	9.0	56
1000	3.80	1.96	9.0	55

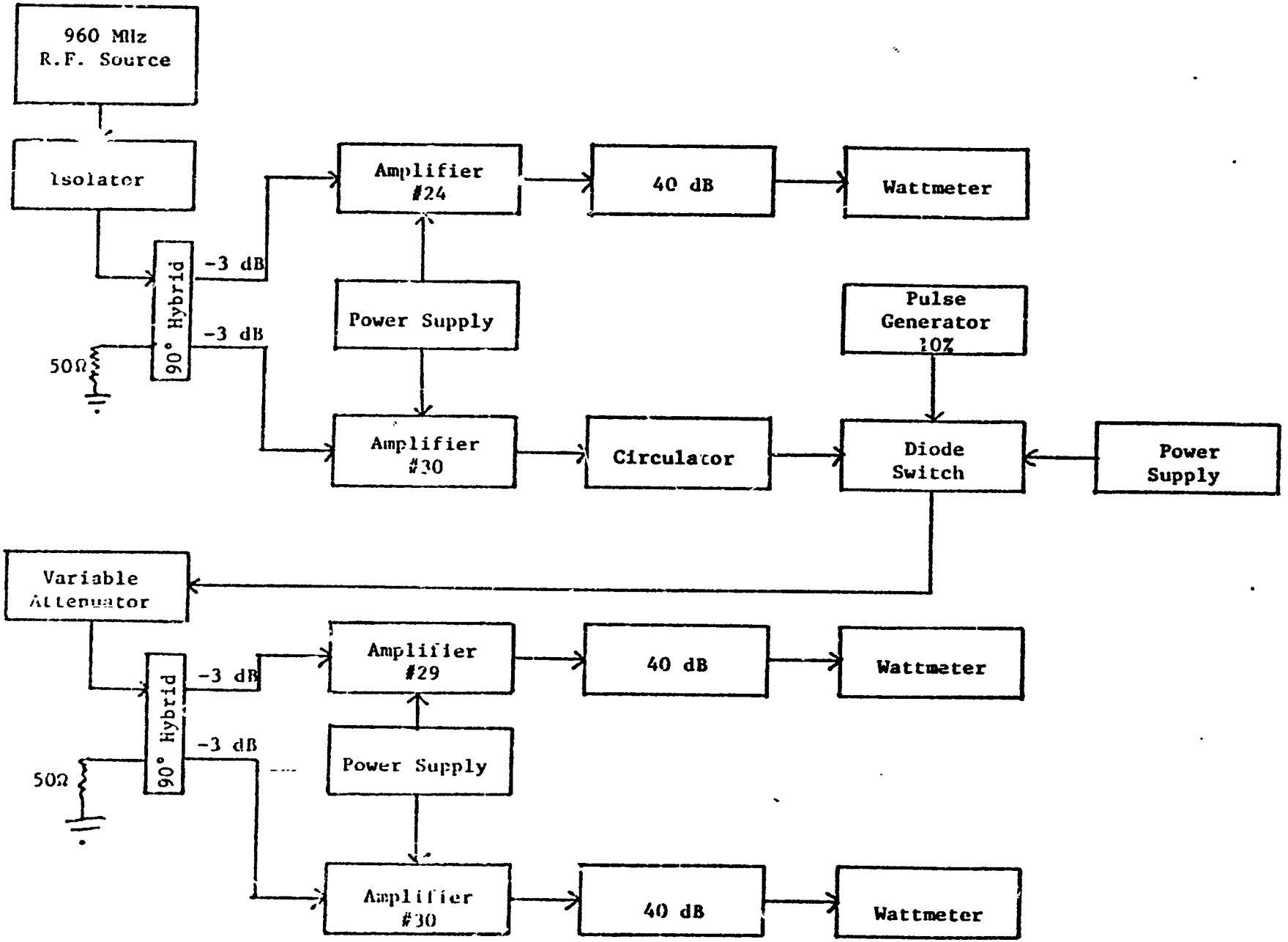


Figure 54. Life Test Setup for Steady State and Intermittent Operation.

TABLE CXV . UNIT #24 PRE LIFE TEST (Steady State) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.72	2.02	9.1	53
650	3.74	2.03	9.0	53
700	3.70	1.99	9.1	54
750	3.82	1.97	9.0	54
800	3.85	1.96	8.9	55
850	3.85	1.98	8.9	54
900	3.87	1.98	8.9	54
950	3.98	2.00	8.8	54
1000	3.96	1.96	8.8	55

TABLE CXVI . UNIT #24 POST LIFE TEST (Steady State) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 22 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.76	2.12	9.0	51
650	3.70	2.11	9.1	51
700	4.22	2.03	8.5	53
750	3.74	2.03	9.0	53
800	3.80	2.04	9.0	53
850	3.84	2.06	8.9	52
900	3.82	2.06	9.0	52
950	3.86	2.03	8.9	53
1000	3.84	2.04	8.9	53

TABLE CXVII . UNIT #27 PRE LIFE TEST (Steady State) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.81	2.03	9.0	53
650	3.74	2.02	9.0	53
700	3.65	1.96	9.1	55
750	3.67	1.91	9.1	56
800	3.67	1.90	9.1	56
850	3.60	1.91	9.2	56
900	3.55	1.91	9.3	56
950	3.72	1.98	9.1	54
1000	3.77	2.00	9.0	54

TABLE CXVIII. UNIT #27 POST LIFE TEST (Steady State) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 21 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.83	2.09	8.9	51
650	3.74	2.08	9.0	52
700	3.64	2.01	9.2	53
750	3.66	1.97	9.1	54
800	3.65	1.96	9.1	55
850	3.57	1.97	9.2	54
900	3.56	1.97	9.3	54
950	3.56	1.96	9.3	55
1000	4.01	2.19	8.7	49

2.12.5.4 Intermittent Life Testing.

Two of the first article amplifiers (#29 and #30) were subjected to intermittent life testing. Figure 54 shows the test setup block diagram. The intermittent testing was done in accordance with Mil-Std-883, Method 1006, condition B. The test conditions were: pulse width = 1 msec, duty cycle = 10%, peak power output = 30 watts, V_{CC} = 28 VDC, T = 80°C., F = 960 MHz, and test duration = 1000 hours. The pretest R. F. data for the two amplifiers is shown in Tables CXIX and CXXI , and after 1000 hours of testing, R. F. data was taken and is shown in Tables CXX and CXXII . A comparison of the pre test and post test R. F. data again reveals no significant changes in performance.

2.12.5.5 Temperature, VSWR, and Overvoltage Tests.

Three of the first article amplifiers (#26, #36, and #37) were subjected to temperature characterization. At ambient operating temperatures of 80°C, 40°C, 0°C, and -40°C, electrical measurements were recorded to determine the thermal effects upon each amplifier's performance. Tables CXXIII through CXXXIV contain the recorded operating conditions of the three amplifiers at the four different temperatures. Tables CXXXV through CXL show the results before and after the tests. Comparing the results of these tables shows that the temperature tests did not significantly alter the operating characteristics of any amplifier.

The same three amplifiers were then subjected to a VSWR test. Each amplifier was turned on while connected to a 3:1 VSWR (3dB pad) terminated in a sliding short and tested at 600MHz and 1000MHz. All phase angles were tested. Data was recorded on the three amplifiers after the VSWR test and is shown in Tables CXLI through CXLIII. No significant performance changes were noted.

TABLE CXIX. UNIT #29 PRE LIFE TEST (Intermittent) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.00	2.06	8.8	52
650	3.79	2.03	9.0	53
700	3.64	1.97	9.1	54
750	3.66	1.94	9.1	55
800	3.61	1.92	9.2	56
850	3.56	1.92	9.3	56
900	3.64	1.93	9.2	56
950	3.90	1.98	8.9	54
1000	4.01	1.94	8.7	55

TABLE CXX . UNIT #29 POST LIFE TEST (Intermittent) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 19 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.18	2.14	8.6	50
650	3.92	2.10	8.8	51
700	3.75	2.04	9.0	53
750	3.70	2.00	9.1	54
800	3.65	1.99	9.1	54
850	3.65	2.00	9.1	54
900	3.75	2.02	9.0	53
950	3.90	2.01	8.9	53
1000	4.37	2.11	8.4	51

TABLE CXXI . UNIT #30 PRE LIFE TEST (Intermittent) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.83	2.06	8.9	52
650	3.60	2.01	9.2	53
700	3.52	1.96	9.3	54
750	3.68	2.00	9.1	54
800	3.71	2.02	9.1	53
850	3.70	2.05	9.1	52
900	3.86	2.04	8.9	53
950	3.90	1.93	8.9	56
1000	3.74	1.82	9.0	59

TABLE CXXII . UNIT #30 POST LIFE TEST (Intermittent) R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 21 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.70	2.13	9.1	50
650	3.52	2.07	9.3	52
700	3.48	2.05	9.4	52
750	3.62	2.06	9.2	52
800	3.60	2.09	9.2	51
850	3.63	2.12	9.2	51
900	3.71	2.11	9.1	51
950	3.61	1.99	9.2	54
1000	3.61	1.92	9.2	56

TABLE CXXIII. UNIT #26 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	4.28	2.26	8.5	47
650	3.96	2.19	8.8	49
700	3.78	2.10	9.0	51
750	3.81	2.06	9.0	52
800	3.95	2.08	8.8	52
850	4.06	2.10	8.7	51
900	4.11	2.12	8.6	51
950	4.25	2.11	8.5	51
1000	4.15	2.02	8.6	53

TABLE CXXIV. UNIT #26 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 40°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 16 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	4.44	2.20	8.3	49
650	4.10	2.14	8.6	50
700	3.86	2.06	8.9	52
750	3.93	2.02	8.8	53
800	4.03	2.03	8.7	53
850	4.06	2.02	8.7	53
900	4.11	2.03	8.6	53
950	4.25	2.03	8.5	53
1000	4.15	1.92	8.6	56

TABLE CXXV . UNIT #26 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 0°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	4.60	2.14	8.1	50
650	4.34	2.12	8.4	51
700	4.03	2.03	8.7	53
750	4.08	1.99	8.7	54
800	4.18	1.99	8.6	54
850	4.23	1.99	8.6	54
900	4.25	1.97	8.5	54
950	4.37	1.97	8.4	54
1000	4.33	1.87	8.4	57

TABLE CXXVI . UNIT #26 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = -40°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 14 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	4.93	2.09	7,8	51
650	4.64	2.09	8.1	51
700	4.28	2.02	8.5	53
750	4.24	1.97	8.5	54
800	4.40	1.97	8.3	54
850	4.48	1.96	8.3	55
900	4.53	1.95	8.2	55
950	4.64	1.94	8.1	55
1000	4.55	1.84	8.2	58

TABLE CXXVII . UNIT #36 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 25 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	3.62	2.10	9.2	51
650	3.45	2.07	9.4	52
700	3.33	2.00	9.5	54
750	3.30	1.95	9.6	55
800	3.37	1.98	9.5	54
850	3.45	2.09	9.4	51
900	3.54	2.12	9.3	51
950	3.57	2.07	9.2	52
1000	3.79	2.14	9.0	50

TABLE CXXVIII.UNIT #36 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 40°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 25 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	3.66	2.04	9.1	53
650	3.53	2.03	9.3	53
700	3.41	1.95	9.4	55
750	3.38	1.90	9.5	56
800	3.41	1.91	9.4	56
850	3.41	1.96	9.4	55
900	3.53	1.99	9.3	54
950	3.57	1.98	9.2	54
1000	3.70	2.00	9.1	54

TABLE CXXIX. UNIT #36 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 0°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 24 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	3.95	2.02	8.8	53
650	3.75	2.00	9.0	54
700	3.62	1.94	9.2	55
750	3.61	1.88	9.2	57
800	3.54	1.88	8.4	57
850	3.62	1.90	9.2	56
900	3.68	1.94	9.1	55
950	3.75	1.93	9.0	56
1000	3.97	2.00	8.8	54

TABLE CXXX . UNIT #36 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = -40°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 23 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	4.23	2.04	8.5	53
650	4.00	1.99	8.8	54
700	3.78	1.92	9.0	56
750	3.77	1.87	9.0	57
800	3.81	1.86	9.0	58
850	3.80	1.88	9.0	57
900	3.89	1.90	8.9	56
950	3.95	1.88	8.8	57
1000	4.01	1.88	8.7	57

TABLE CXXXI . UNIT #37 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	3.78	2.14	9.0	50
650	3.57	2.06	9.2	52
700	3.49	2.00	9.3	54
750	3.61	1.97	9.2	54
800	3.65	1.97	9.1	54
850	3.52	1.98	9.3	54
900	3.58	2.00	9.3	54
950	3.72	2.03	9.1	53
1000	3.70	1.97	8.6	54

TABLE CXXXII . UNIT #37 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 40°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	3.95	2.08	8.8	52
650	3.70	2.01	9.1	53
700	3.62	1.93	9.2	56
750	3.65	1.90	9.1	56
800	3.74	1.90	9.0	56
850	3.66	1.89	9.1	57
900	3.61	1.89	9.2	57
950	3.72	1.91	9.1	56
1000	3.65	1.82	9.1	59

TABLE CXXXIII. UNIT #37 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = 0°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	4.15	2.04	8.6	53
650	3.92	1.99	8.8	54
700	3.78	1.90	9.0	56
750	3.85	1.86	8.9	58
800	3.92	1.87	8.8	57
850	3.87	1.84	8.9	58
900	3.82	1.85	9.0	58
950	3.91	1.84	8.8	58
1000	3.79	1.76	9.0	61

TABLE CXXXIV. UNIT #37 PERFORMANCE DATA IN ENVIRONMENTAL CHAMBER T = -40°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 19 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)
600	4.36	2.06	8.4	52
650	4.09	1.98	8.7	54
700	3.95	1.90	8.8	56
750	4.00	1.85	8.8	58
800	4.1	1.85	8.6	58
850	4.04	1.83	8.7	59
900	4.00	1.82	8.8	59
950	4.07	1.81	8.7	59
1000	4.01	1.73	8.7	62

TABLE CXXXV. UNIT #26 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 14 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	4.35	2.13	8.4	50	- 40
650	4.01	2.09	8.7	51	-113
700	3.85	2.02	8.9	53	167
750	3.99	2.00	8.8	54	86
800	4.04	1.98	8.7	54	5
850	4.04	1.99	8.7	54	- 75
900	4.08	1.99	8.7	54	-156
950	4.27	2.01	8.4	53	122
1000	4.39	1.96	8.3	55	37

TABLE CXXXVI . UNIT #36 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 15 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.69	2.00	9.1	54	- 41
650	3.56	1.96	9.2	55	-114
700	3.41	1.87	9.4	57	165
750	3.35	1.84	9.5	58	83
800	3.42	1.86	9.4	58	0
850	3.45	1.96	9.4	55	- 86
900	3.56	1.98	9.2	54	-169
950	3.53	1.92	9.2	56	112
1000	3.49	1.86	9.3	58	26

TABLE CXXXVII . UNIT #37 PERFORMANCE DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (ADC)	Gain (dB)	η (%)	Phase Relative (Degrees)
600	3.84	2.04	8.9	53	- 33
650	3.60	1.95	9.2	55	-113
700	3.52	1.91	9.3	56	163
750	3.20	1.89	9.1	56	82
800	3.70	1.86	9.1	58	8
850	3.56	1.84	9.2	58	- 80
900	3.50	1.84	9.3	58	-164
950	3.74	1.90	9.0	56	110
1000	3.80	1.86	9.0	58	18

TABLE CXXXVIII. UNIT #26 PRE 3:1 VSWR AND OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 13 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.55	2.14	8.2	50
650	4.09	2.12	8.7	51
700	4.01	2.04	8.7	53
750	4.27	2.00	8.5	54
800	4.66	1.99	8.1	54
850	4.80	1.99	8.0	54
900	4.22	1.97	8.5	54
950	3.94	1.95	8.9	55
1000	4.25	1.90	8.5	56

TABLE CXXXIX. UNIT #28 PRE 3:1 VSWR AND OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 25 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.76	2.02	9.0	53
650	3.65	2.02	9.1	53
700	3.49	1.94	9.3	55
750	3.49	1.88	9.3	57
800	3.49	1.88	9.3	57
850	3.50	1.90	9.3	56
900	3.60	1.96	9.2	55
950	3.67	1.96	9.1	55
1000	3.61	1.92	9.2	56

TABLE CXL . UNIT #26 PRE 3:1 VSWR TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 13 dB.

f (Mlz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.54	1.96	8.2	55
650	4.26	2.11	8.5	51
700	4.01	2.03	8.7	53
750	4.03	1.99	8.7	54
800	4.13	1.98	8.6	54
850	4.17	1.98	8.6	54
900	4.21	1.98	8.5	54
950	4.23	1.94	8.5	55
1000	4.21	1.91	8.5	56

TABLE CXLI . UNIT #26 POST 3:1 VSWR TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 13 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.54	1.96	8.2	55
650	4.26	2.11	8.5	51
700	4.01	2.03	8.7	53
750	4.03	1.99	8.7	54
800	4.13	1.98	8.6	54
850	4.17	1.98	8.6	54
900	4.21	1.98	8.5	54
950	4.23	1.94	8.5	55
1000	4.21	1.91	8.5	56

TABLE CXLII UNIT #36 POST 3:1 VSWR TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 25 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.76	2.01	9.0	53
650	3.62	2.02	9.2	53
700	3.48	1.93	9.4	56
750	3.49	1.88	9.3	57
800	3.49	1.88	9.3	57
850	3.50	1.90	9.3	54
900	3.60	1.96	9.2	55
950	3.66	1.96	9.1	55
1000	3.61	1.90	9.2	56

TABLE CXLIII. UNIT #37 POST 3:1 VSWR TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.01	2.06	8.7	52
650	3.80	1.99	9.0	54
700	3.68	1.90	9.1	56
750	3.77	1.87	9.0	57
800	3.82	1.86	9.0	58
850	3.74	1.85	9.0	58
900	3.73	1.84	9.1	58
950	3.74	1.83	9.0	59
1000	3.77	1.80	9.0	60

Finally an overvoltage test was performed on the same three amplifiers. V_{CC} was raised from 28 volts to 30 volts and R. F. data was recorded. Then the voltage was reduced back to 28 volts and performance data again recorded. This data is shown in Tables CXLIV thru CXLIX. Again, no significant performance changes occurred.

Since no real changes in operating characteristics occurred during or after the three environmental tests, the integrity of the overall design is good. Future production runs will survive these environments, as long as the processing is controlled.

2.12.5.6 Sealing.

Three first article amplifiers were successfully weld sealed by Microwave Associates after some difficulty. Previous attempts to effect a hermetic weld seal failed due to side wall overheating causing leaks to appear at the RF connectors or B+ feedthru capacitors. After return of amplifiers 41, 42, and 43 from sealing, gross leak tests were performed and all the housings passed.

Next the amplifiers were subjected to the radioisotope fine leak test per Mil-Std-883, Method 1014, Condition B. These tests were performed by Trio-Tech, Inc. using the radioisotope fine leak test process of bombing the housings with Krypton-85 radioactive gas (34PSi) for a period of 12 minutes. After exposure, the housings are removed and examined for radiation which indicates a leak exists. The leak rates for amplifiers 41, 42, and 43 were 1.5, 2.0, and 1.5 thousand counts per minute (CPM) respectively. The leak rates for amplifiers 41, 42, and 43 were 1.5, 2.0, and 1.5 x 10^{-7} atm cc/sec of Krypton-85 respectively. This is an excellent seal for a housing of this size. After the leak testing, R. F. data was taken on each amplifier and compared with the pre leak

TABLE CXVIV. UNIT #26 OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 30V, RETURN LOSS = > 13 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.35	2.12	8.4	47
650	4.15	2.12	8.6	47
700	3.88	2.04	8.9	49
750	3.98	1.99	8.8	50
800	4.04	1.97	8.7	51
850	4.06	1.97	8.7	51
900	4.09	1.96	8.7	51
950	4.13	1.92	8.6	52
1000	4.11	1.87	8.6	53

TABLE CXLV . UNIT #26 POST OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 13 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.56	2.16	8.2	50
650	4.24	2.12	8.5	51
700	4.01	2.04	8.7	53
750	4.03	2.01	8.7	53
800	4.10	2.00	8.6	54
850	4.15	2.00	8.6	54
900	4.20	2.00	8.5	54
950	4.23	1.95	8.5	55
1000	4.23	1.91	8.5	56

TABLE CXLVI . UNIT #36 OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 30V, RETURN LOSS = > 25 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.66	2.00	9.1	50
650	3.61	2.01	9.1	50
700	3.47	1.92	9.4	52
750	3.44	1.86	9.4	54
800	3.42	1.85	9.4	54
850	3.41	1.86	9.4	54
900	3.44	1.88	9.4	53
950	3.54	1.90	9.3	53
1000	3.46	1.83	9.4	55

TABLE CXLVII . UNIT #36 OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 25 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.79	2.02	9.0	53
650	3.65	2.02	9.1	53
700	3.49	1.94	9.3	55
750	3.49	1.88	9.3	57
800	3.49	1.88	9.3	57
850	3.48	1.90	9.3	54
900	3.59	1.95	9.2	55
950	3.66	1.96	9.1	55
1000	3.61	1.91	9.2	56

TABLE CXLVIII. UNIT #37 OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 30V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.92	2.05	8.8	49
650	3.74	1.91	9.0	52
700	3.66	1.91	9.1	52
750	3.73	1.87	9.1	53
800	3.76	1.84	9.0	54
850	3.71	1.83	9.1	55
900	3.61	1.82	9.2	55
950	3.62	1.80	9.2	56
1000	3.63	1.76	9.2	57

TABLE CXLIX. UNIT #37 POST OVERVOLTAGE TEST R.F. DATA T = 25°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 20 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.02	2.06	8.7	52
650	3.80	1.99	9.0	54
700	3.68	1.92	9.1	56
750	3.81	1.88	9.0	57
800	3.82	1.87	9.0	57
850	3.72	1.86	9.1	58
900	3.71	1.85	9.1	58
930	3.74	1.84	9.0	58
1000	3.80	1.82	9.0	59

test R. F. data. See Table CL through CLV for the data. No significant changes in performance were measured.

2.12.5.7 Temperature Cycling and Thermal Shock.

Temperature cycling tests were performed on amplifiers 41, 42, and 43 per Mil-Std-883, Method 1010, Condition B, 5 cycles. These tests were done at TRW Semiconductors using temperature test points of -55°C, 25°C, and 125°C per Condition B of the Mil specification. After five cycles of testing, the three amplifiers were then exposed to thermal shock tests per Mil-Std-883, Method 1011, Condition A, 5 cycles. These tests were also done at TRW Semiconductors and the thermal shock temperature extremes were 0°C and 100°C. Water mixed with ice provided 0°C and boiling water yielded the 100°C extreme. After these tests, gross and fine leak tests were made on the amplifiers as detailed in Section 2.12. 5.6. Immediately following, R. F. data was recorded on the three amplifiers and compared with the pre temperature cycling and thermal shock test data. See Tables CLVI through CLVIII. A fine leak test performed after these tests showed no change in the previously (Secton 2.12.5.7) measured leak rates.

2.12.5.8 Moisture Resistance

Amplifiers 41, 42, and 43 were lastly subjected to a moisture resistance test per Mil-Std-883 with the initial conditioning omitted. This test was performed at TRW Semiconductors. A graphical representation of the test is shown in Appendix A. R. F. data was recorded following the moisture resistance test and is shown in Tables CLIX through CLXI. No significant performance changes we recorded indicating the overall insensitivity of the amplifier module to the effects of moisture. Figure 55 graphically describes the moisture resistance test profile.

TABLE CL . UNIT #41 PRE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 17 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.94	1.98	8.8	54
650	3.62	1.99	9.2	54
700	3.50	1.97	9.3	54
750	3.47	1.96	9.4	55
800	3.53	1.96	9.3	55
850	3.57	1.97	9.2	54
900	3.65	1.97	9.1	54
950	3.66	1.96	9.1	55
1000	3.70	2.00	9.1	54

TABLE CLI . UNIT #42 PRE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 16 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.18	1.95	8.6	55
650	3.88	1.95	8.9	55
700	3.70	1.92	9.1	56
750	3.69	1.93	9.1	56
800	3.79	1.96	9.0	55
850	3.93	2.00	8.8	54
900	3.97	1.99	8.8	54
950	4.09	1.97	8.7	54
1000	4.20	2.02	8.5	53

TABLE CLII . UNIT #43 PRE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 17 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.14	2.03	8.6	53
650	3.73	2.00	9.1	54
700	3.55	1.97	9.3	54
750	3.65	1.99	9.1	54
800	3.83	2.00	8.9	54
850	4.01	2.01	8.7	53
900	4.13	2.02	8.6	53
950	4.18	1.98	8.6	54
1000	4.20	2.04	8.5	53

TABLE CLIII. UNIT #41 POST FINE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.79	1.96	9.0	55
650	3.52	1.99	9.3	54
700	3.40	1.96	9.5	55
750	3.39	1.95	9.5	55
800	3.40	1.95	9.3	55
850	3.50	1.94	9.3	55
900	3.51	1.95	9.3	55
950	3.60	1.94	9.2	55
1000	3.65	2.00	9.1	54

TABLE CLIV. UNIT #42 POST FINE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 16 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.14	1.99	8.6	54
650	3.88	1.98	8.9	54
700	3.72	1.94	9.1	55
750	3.65	1.94	9.1	55
800	3.74	1.96	9.0	55
850	3.85	1.98	8.9	54
900	3.89	1.96	8.9	55
950	3.87	1.91	8.9	56
1000	4.15	2.02	8.6	53

TABLE CLV . UNIT #43 POST FINE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 17 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.09	2.01	8.7	53
650	3.71	1.99	9.1	54
700	3.55	1.95	9.3	55
750	3.63	1.96	9.2	55
800	3.79	1.99	9.0	54
850	3.97	2.00	8.8	54
900	4.11	2.00	8.6	54
950	4.13	1.96	8.6	55
1000	4.10	1.98	8.6	54

TABLE CLVI . UNIT #41 POST TEMPERATURE CYCLING, THERMAL SHOCK, AND FINE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 17 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.99	1.97	8.8	54
650	3.73	1.99	9.1	54
700	3.60	1.96	9.2	55
750	3.60	1.96	9.2	55
800	3.70	1.96	9.1	55
850	3.69	1.95	9.1	55
900	3.73	1.95	9.1	55
950	3.79	1.94	9.0	55
1000	3.85	2.00	8.9	54

TABLE CLVII . UNIT #42 POST TEMPERATURE CYCLING, THERMAL SHOCK, AND FINE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 16 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.45	2.00	8.3	54
650	4.12	1.99	8.6	54
700	3.95	1.94	8.8	55
750	3.88	1.94	8.9	55
800	4.00	1.97	8.8	54
850	4.09	1.98	8.7	54
900	4.09	1.96	8.7	55
950	4.13	1.91	8.6	56
1000	4.30	2.01	8.4	53

TABLE CLVIII. UNIT #43 POST TEMPERATURE CYCLING, THERMAL SHOCK, AND FINE LEAK TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 17 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.32	2.03	8.4	53
650	3.91	2.00	8.8	54
700	3.75	1.97	9.0	54
750	3.83	1.99	8.9	54
800	4.04	2.00	8.7	54
850	4.17	2.01	8.6	53
900	4.31	2.00	8.4	54
950	4.35	1.97	8.4	54
1000	4.35	1.98	8.4	54

TABLE CLIX. UNIT #41 POST MOISTURE RESISTANCE TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	3.79	1.99	9.0	54
650	3.54	2.00	9.4	54
700	3.45	1.97	9.4	54
750	3.42	1.96	9.4	55
800	3.53	1.96	9.3	55
850	3.53	1.95	9.3	55
900	3.53	1.95	9.0	55
950	3.79	1.93	9.0	56
1000	3.65	2.00	9.1	54

TABLE CLX . UNIT #42 POST MOISTURE RESISTANCE TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 16 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.25	2.00	8.5	54
650	3.93	1.99	8.8	54
700	3.75	1.95	9.0	55
750	3.74	1.96	9.0	55
800	3.83	1.98	8.9	54
850	3.89	1.98	8.9	54
900	3.96	1.95	8.8	55
950	3.96	1.92	8.8	56
1000	4.18	2.02	8.6	53

TABLE CLXI . UNIT #43 POST MOISTURE RESISTANCE TEST R.F. DATA T = 80°C, P_{OUTPUT} = 30W, V_{CC} = 28V, RETURN LOSS = > 18 dB.

f (MHz)	P_{IN} (Watts)	I_C (Amps)	GAIN (dB)	η (%)
600	4.07	2.00	8.7	54
650	3.67	1.98	9.1	54
700	3.55	1.96	9.3	55
750	3.65	1.98	9.1	54
800	3.83	2.00	8.9	54
850	3.97	2.01	8.8	53
900	4.13	2.01	8.6	53
950	4.18	1.97	8.6	54
1000	4.15	2.00	8.6	54

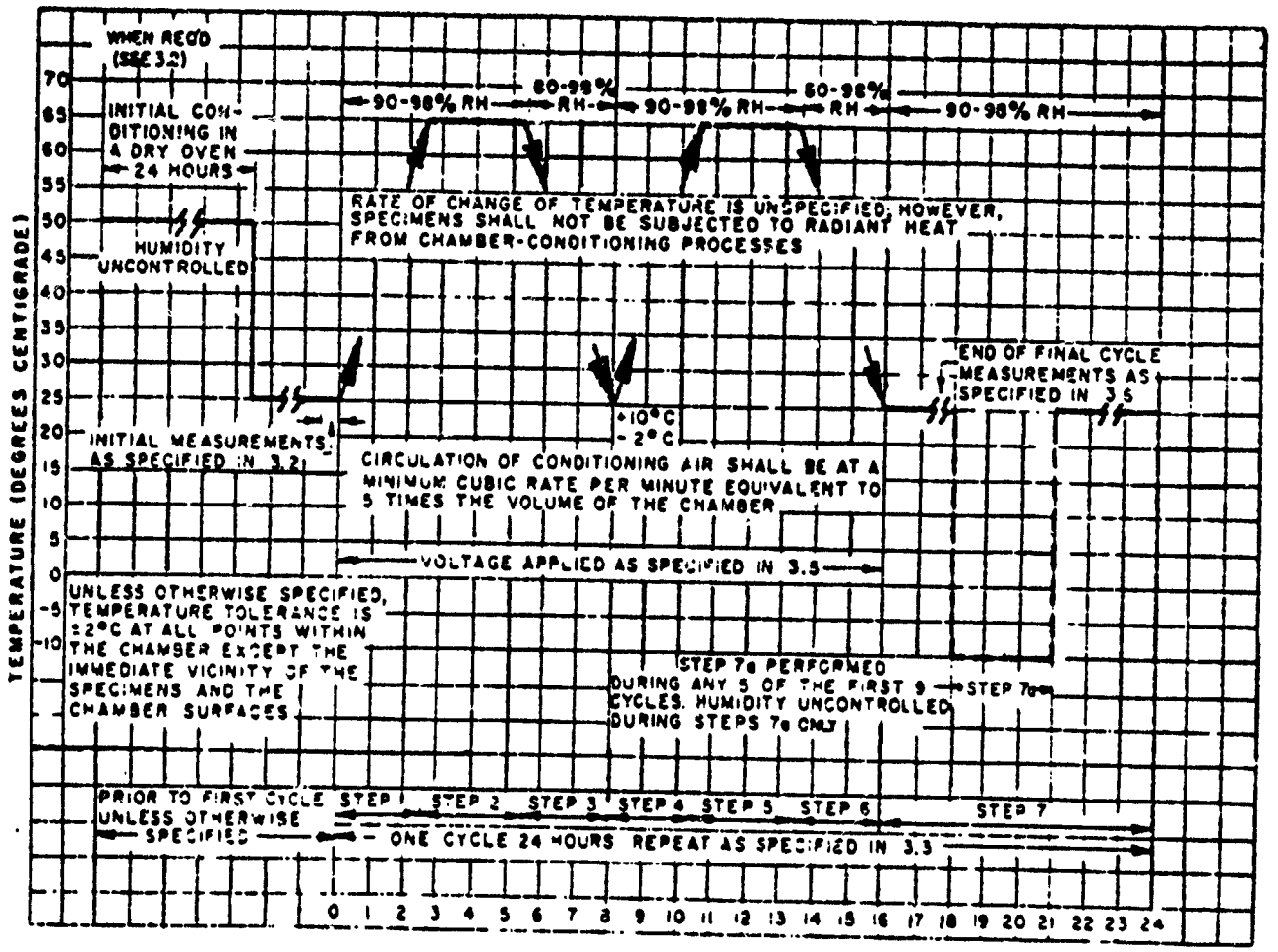


Figure 55. Graphical Representation of Moisture-resistance Test.